

## SHEET

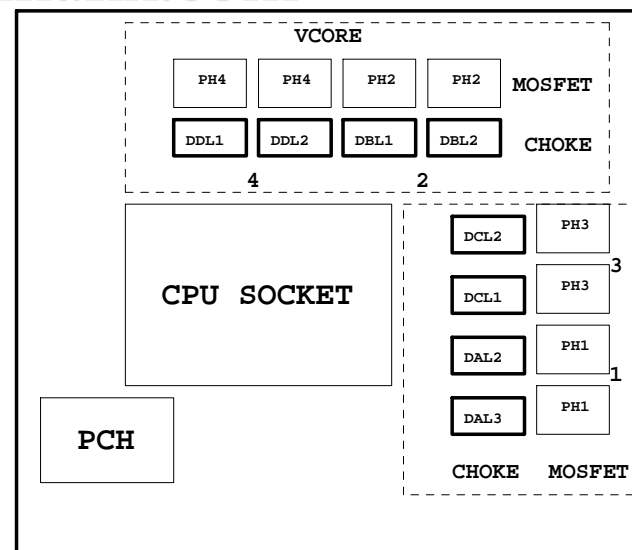
## TITLE

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03	BLOCK DIAGRAM
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05	CPU_LGA1150-B
06	CPU_LGA1150-C
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08	DDR III CHANNEL B
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11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
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16	PCI EXPRESS*16 SWITCH
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26	VCORE_ ISL95820_1
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## SHEET

## TITLE

29	NCP3933 OVER VOLTAGE
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31	F_PANEL , F_USB2.0/3.0
32	ATX POWER, CLOCK GEN
33	HWM , KB/MS , FAN CTRL
34	Bigfoot E2201
35	DP / HDMI
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Gigabyte Technology

Title			
Cover Sheet			
Size	Document Number	G1.Sniper Z97	
Custom			Rev 1.11
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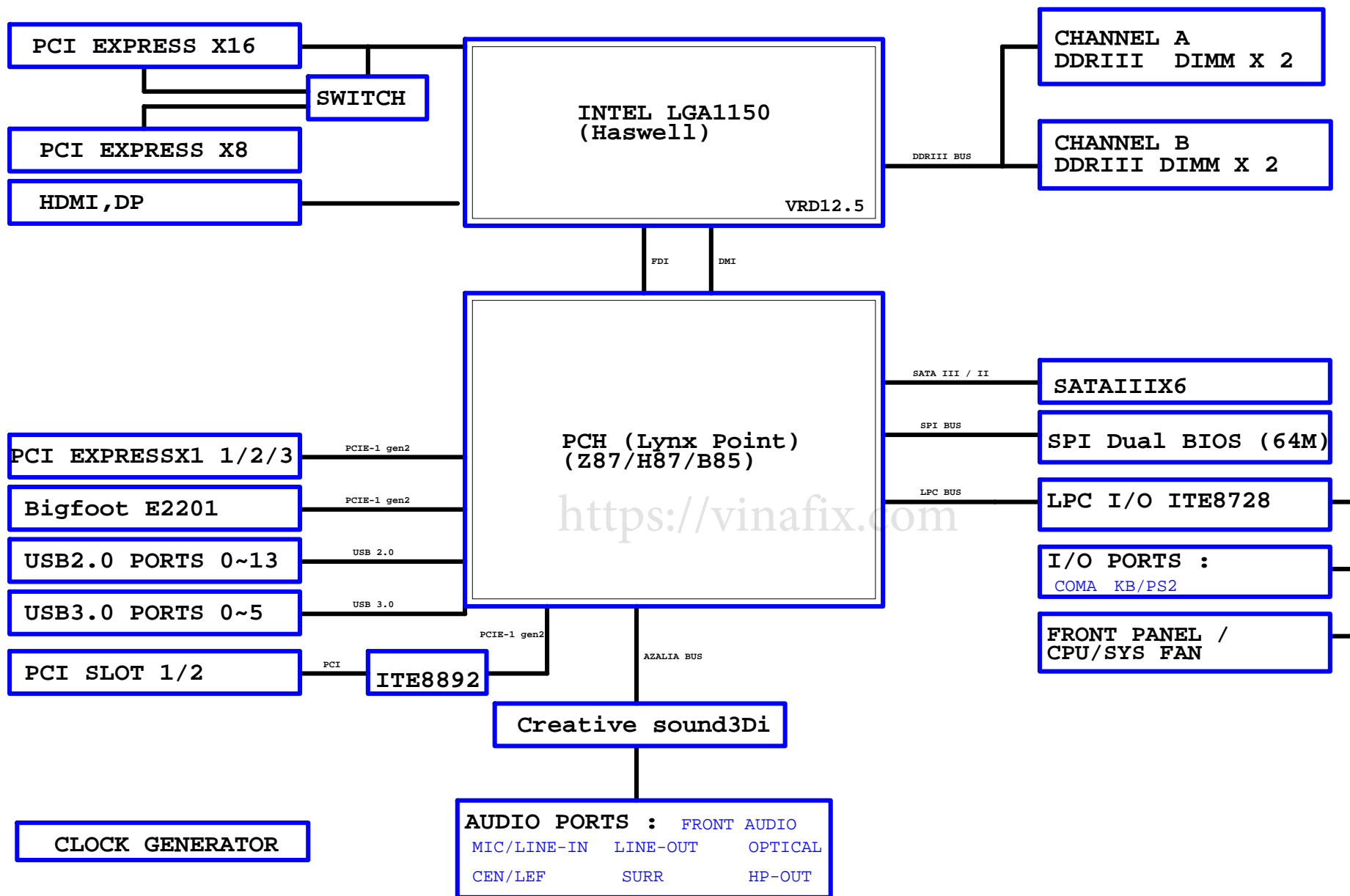
**Model Name: G1.Sniper Z97**

## Component value change history

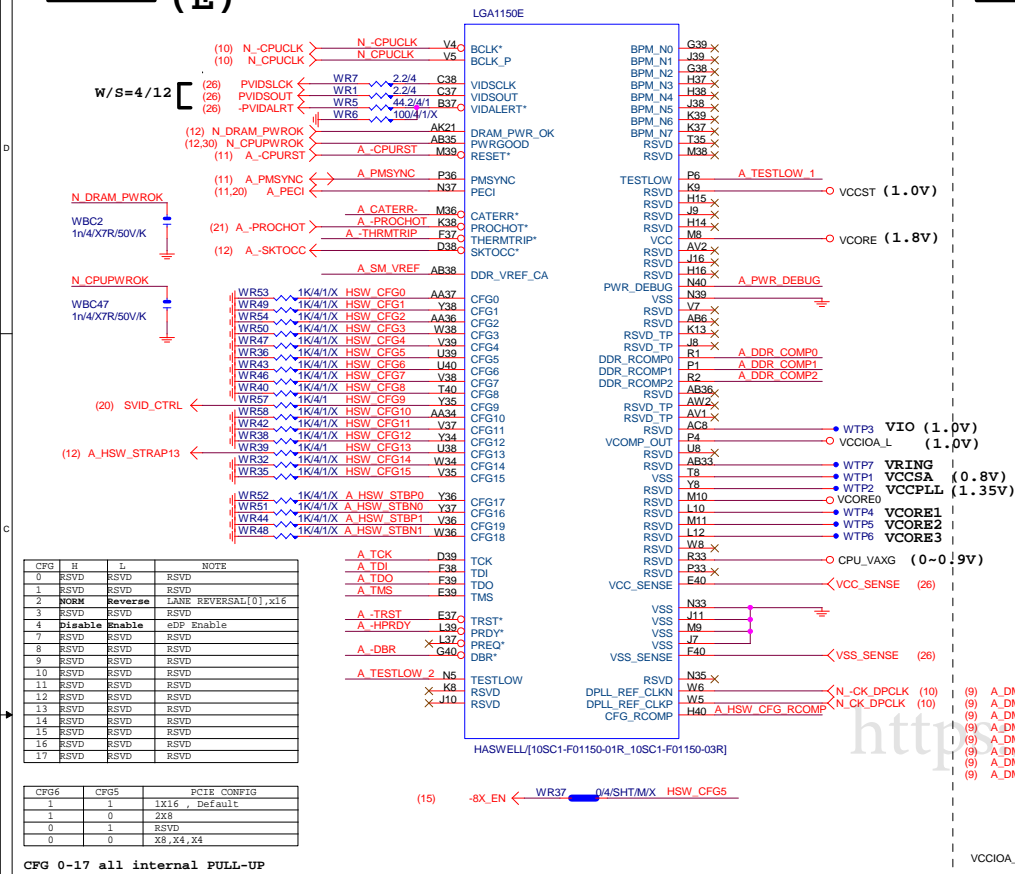
## Circuit or PCB layout change

DATE	Change Item	Reason
2013/07/31	1.由Z87X-HD3 Rev 0.1來修改 2.Remove RGB&DVI 3.Add HDMI&DP 4.Add 直立式USB2.0 port and 獨立power 5.Remove F_USB3 6.Add Power,reset,...button 7.Audio change to creative 8.LAN change to E2201	Rev 0.1
2013/09/05	1.由G1.Sniper Z87 Rev 0.1來修改 2.MBIOS_LED靠近M_BIOS 3.BBIOS_LED 靠近B_BIOS 4.Add CR152 靠近MOAT3 5.CU7 Pin19,CR18,CBC57 改接GND 6.新增DR169 7.新增MOS保護線路, RS2 請靠近DCQ5 8.DACC4,DACC5 footprint 改為C0805 9.PPAK footprint改為Q_TDS0N8-GDS-T 10. POLYSWITCH-1206 改為POLYSWITCH-1206-1	Rev 0.2
2013/09/27	1.由G1.Sniper Z87 Rev 0.2來修改 2.VCCIO2PCH 請加粗至20MIL 3.ADD NC 60 .請靠近NR51 4.CBC21 改AGND 5.R676改0603 6.NCT3941 foot print 改SOP8-NCT3941S 7.修改USB DAC 線路 8.BIOS LED移開些	Rev 1.0
2013/09/27	1.由G1.Sniper Z87 Rev 1.1來修改 2.修改BIOS_sw跟SB線路	Rev 1.11
2014/02/13	1. 修改model name 為G1.Sniper Z97 2. PCH_HS修改為BGAHSINK-G1-A85X-PCH-1	Rev 1.0
2014/05/02	1. Fix Audio POP noise 2. Fix USB_DAC S3 issue 3. 0 ohm change to short pad	Rev 1.1
2014/06/20	1. SATA MLCC change to short pad 2. UBE4 pin 1極性標示	Rev 1.11

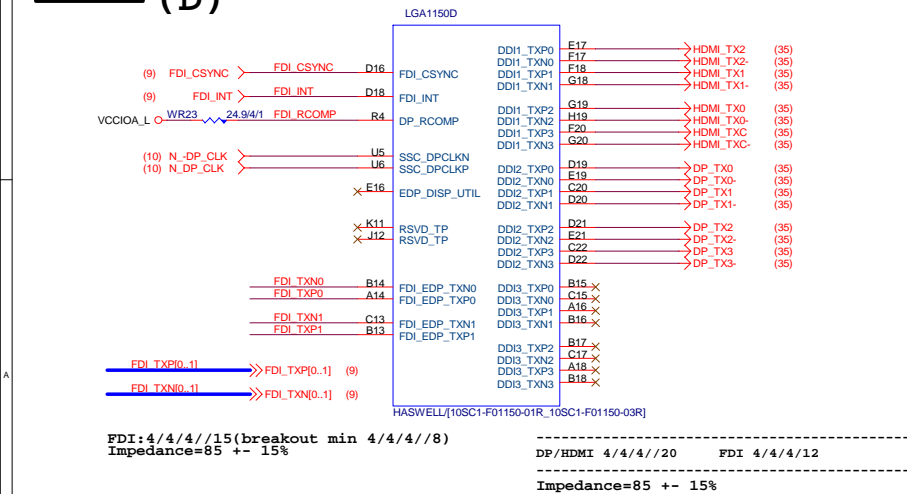
# BLOCK DIAGRAM



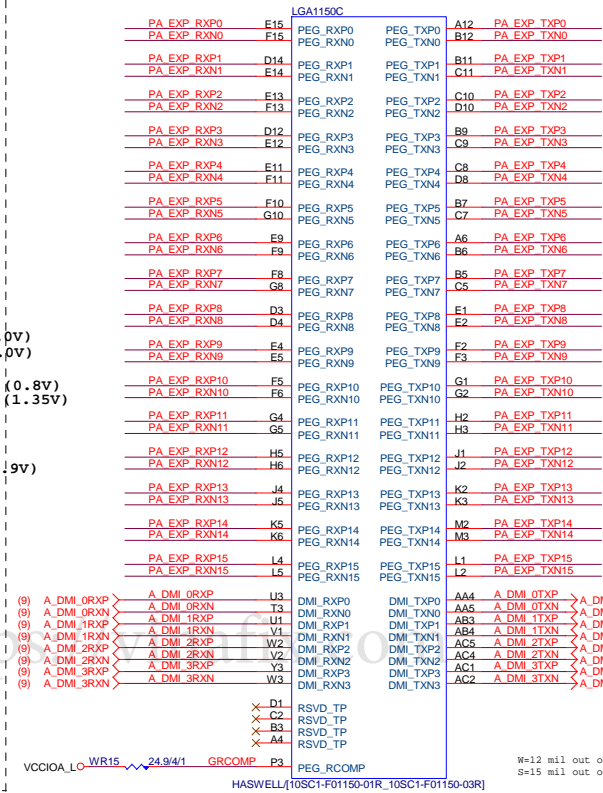
LGA1150 (E)



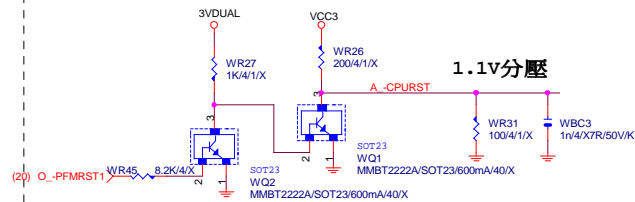
**LGA1150 (D)**



LGA1155 (C)



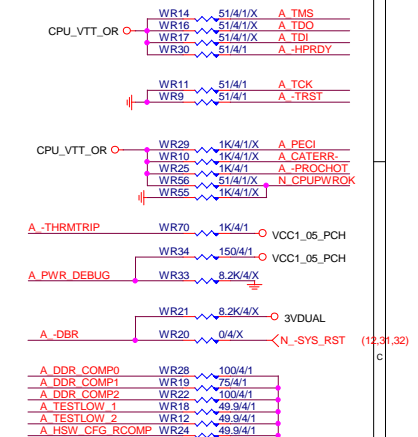
## -CPURST



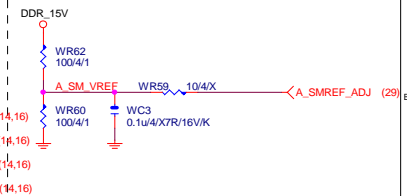
## CPU SVID



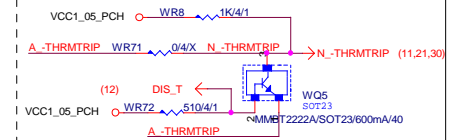
## CPU PU/PD



## SM REF



THRMTRIP DISABLE FOR Z87 OVERCLOCK



## Gigabyte Technology

**CPU LGA1150-A**

## G1.Sniper Z97

1.11

(A)

LGA1150A

HASWELL/I10SC1-F01150-01R I10SC1-F01150-03R1

(B)

LGA1150B

HASWELL/I10SC1-F01150-01R I10SC1-F01150-03R

(CR)

ILM BP CR/115X/BKNI

## DDR BUS

(7) MODT\_A[0..3]  $\leftrightarrow$  MODT\_A[0..3]  
(8) MODT\_B[0..3]  $\leftrightarrow$  MODT\_B[0..3]

(7) MDA[0..63]  $\leftrightarrow$  MDA[0..63]  
(8) MDB[0..63]  $\leftrightarrow$  MDB[0..63]

(7) DQSA[0..7]  $\leftrightarrow$  DQSA[0..7]  
(8) -DQSA[0..7]  $\leftrightarrow$  -DQSA[0..7]

(7) MAAA[0..15]  $\leftrightarrow$  MAAA[0..15]  
(8) MAAB[0..15]  $\leftrightarrow$  MAAB[0..15]

(7) DQSB[0..7]  $\leftrightarrow$  DQSB[0..7]  
(8) -DQSB[0..7]  $\leftrightarrow$  -DQSB[0..7]

## Gigabyte Technology

Title			
CPU LGA1150-B			
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(F, J)



(G,H,I)



(X30)

(X15)



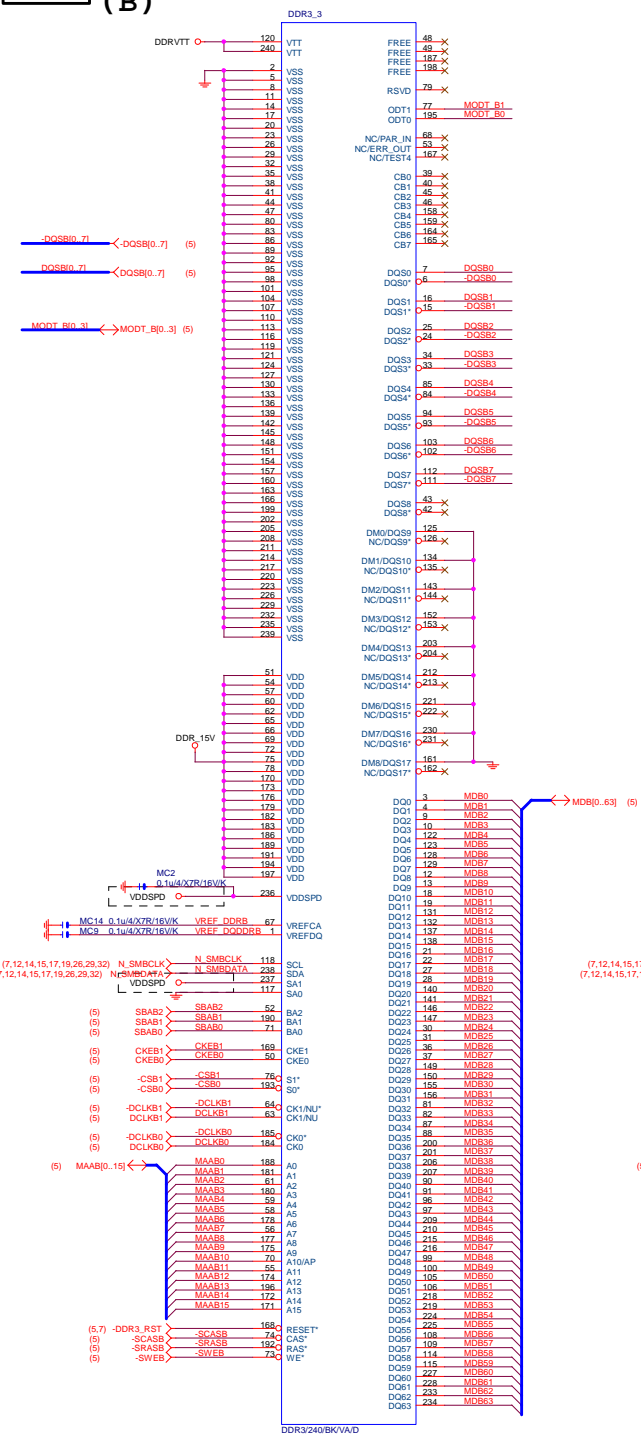
Rev	
1 1	

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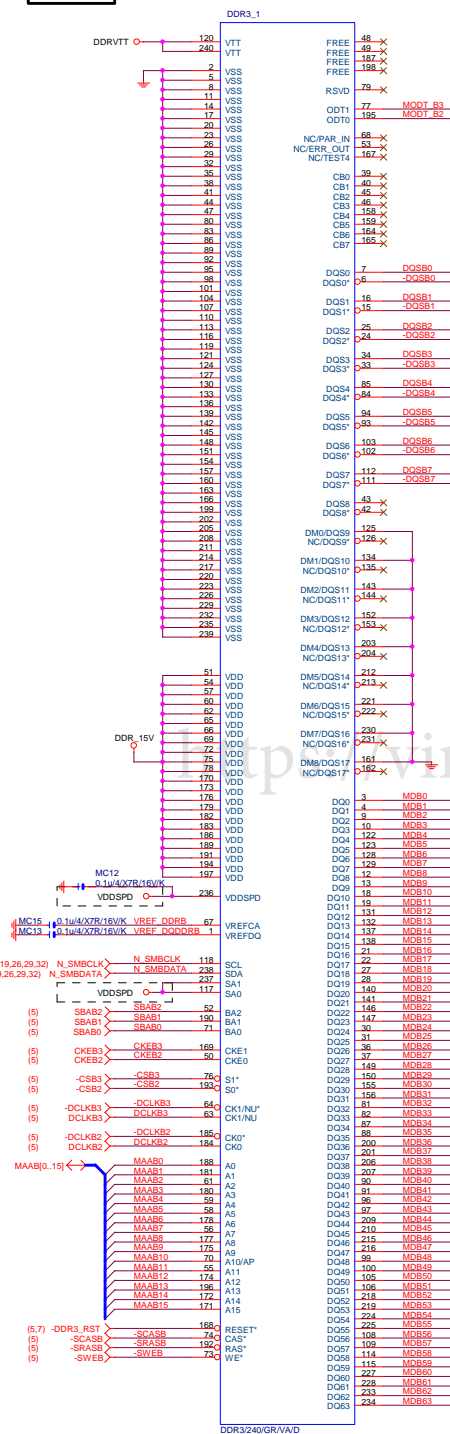


DDR3

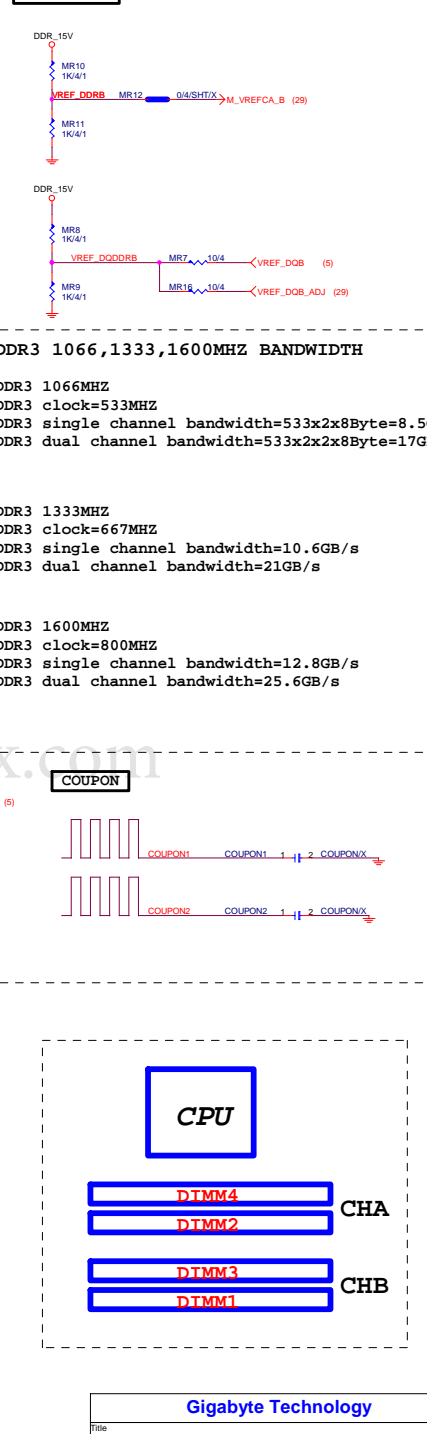
(B)



DDR3



DDR3 VREF



DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ  
DDR3 clock=533MHZ  
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s  
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

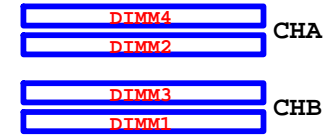
DDR3 1333MHZ  
DDR3 clock=667MHZ  
DDR3 single channel bandwidth=10.6GB/s  
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ  
DDR3 clock=800MHZ  
DDR3 single channel bandwidth=12.8GB/s  
DDR3 dual channel bandwidth=25.6GB/s

COUPON



CPU



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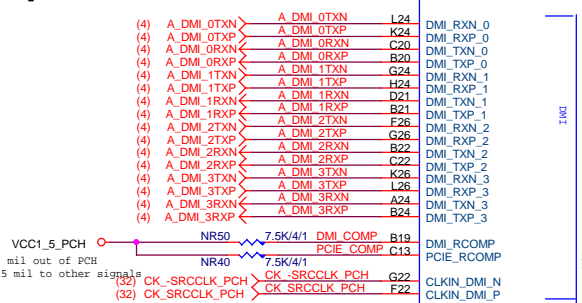
Title			DDR3 CHANNEL B
Size			Document Number
Custom			G1.Sniper Z97
Date			Rev 1.11

PCH

(B)

DMI:12/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)  
Impedance=85 +- 15%



REAR USB3.0

LAN AR8161

ITE8892 PCI

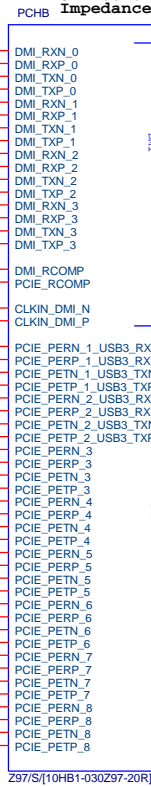
Bridge

PCIEX1

PCIEX1

PCIEX1

放靠近 Device &amp; PCI-E Slot



PCH PCIE ,DMI 4/4/4//15 Impedance=85 +- 15%

usb2.0 5/7/5//12 Impedance=85 +- 15%

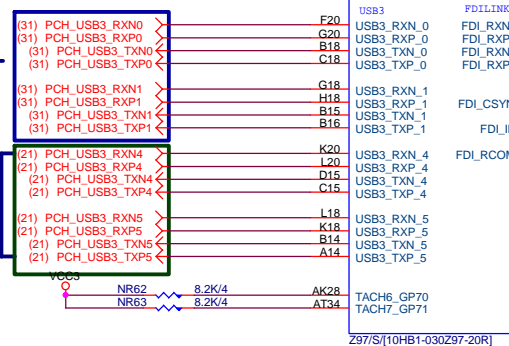
usb3.0 5/7/5//20

PCH

(F)

Port要對應

B85/H81: 5/7 N/A  
B85/H81: 5/7 N/A  
H81:USB3.0 N/A  
H81:12/13 N/A



USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS

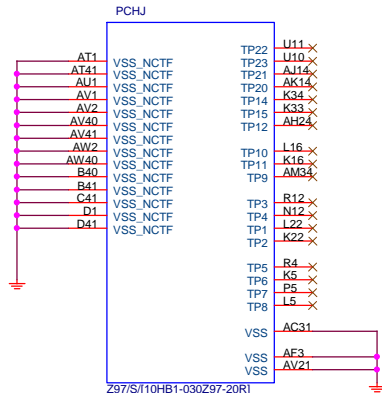
CK\_SRCCLK\_PCH NR89 8.2K/4  
CK\_SRCCLK\_PCH NR88 8.2K/4

Mount for integrated clock Generation Mode

CK\_DOTCLK NR92 8.2K/4  
CK\_DOTCLK NR91 8.2K/4  
NR92 short to GND in non graphic SKU

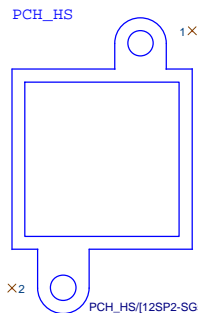
PCH

(J)



PCH H/S

PCH\_HS



PCH\_HS[12SP2-SG5574-11R\_12SP2-SG5574-12R\_12SP2-SG5574-13R]

USB TABLE

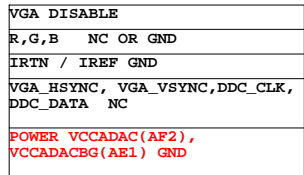
OC[3:0]# for Device 29 (ports 0-7)  
OC[7:4]# for Device 26 (ports 8-13)

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

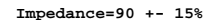
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Title					Rev 1.1
PCH FDI,DMI,USB ,PCIE					
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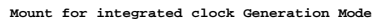
(E)



(G)



PCH	CLK	PD
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## VGA DDC

## VGA ESD

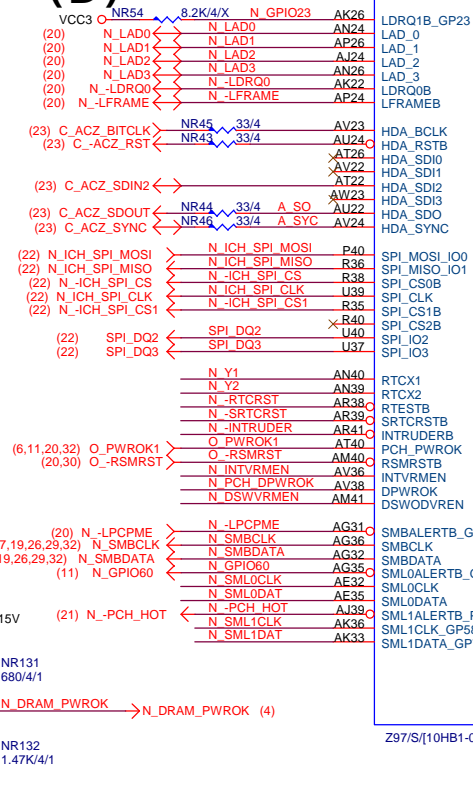
## VGA DDC

## VGA CONNECTOR



## PCH

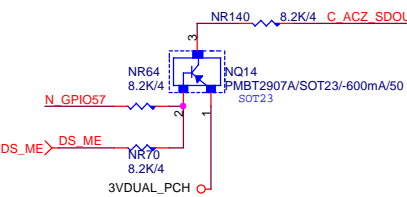
(D)



Vinafix.com

## ACZ\_SDOUT

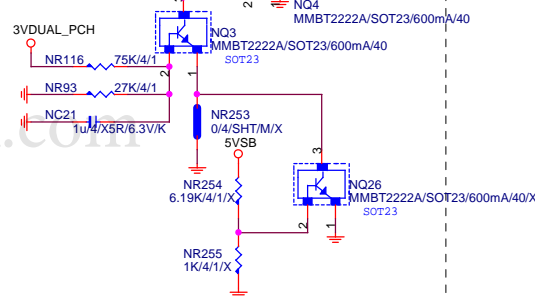
C\_ACZ\_SDOUT : HI --> ME Enable  
 Lo --> ME Disable  
 HI: disable ME and override SPI Flash Access Permissions



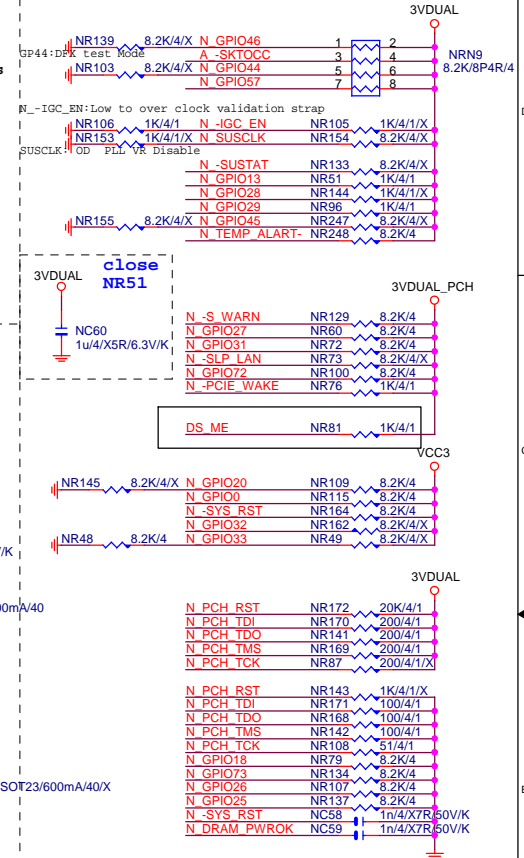
## PCH\_DPWROK

At least 10ms delay after 3VDUAL\_PCH stabel

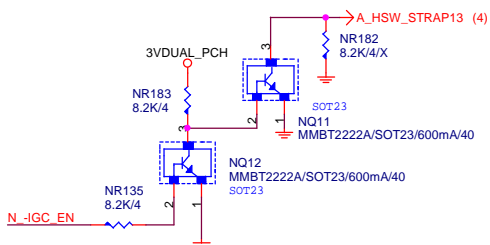
At least 40ns lead fall to 0V before 3VDUAL\_PCH fall to 2V



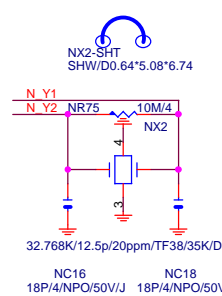
## PCH PU/PD



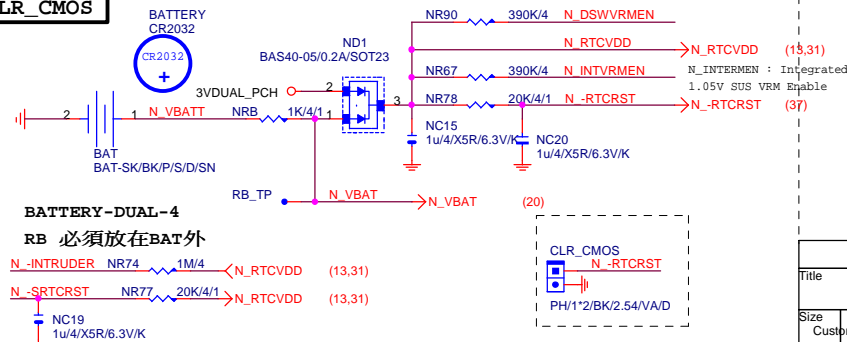
## HSW\_STRAP13



## 32.768KHZ



## CLR\_CMOS



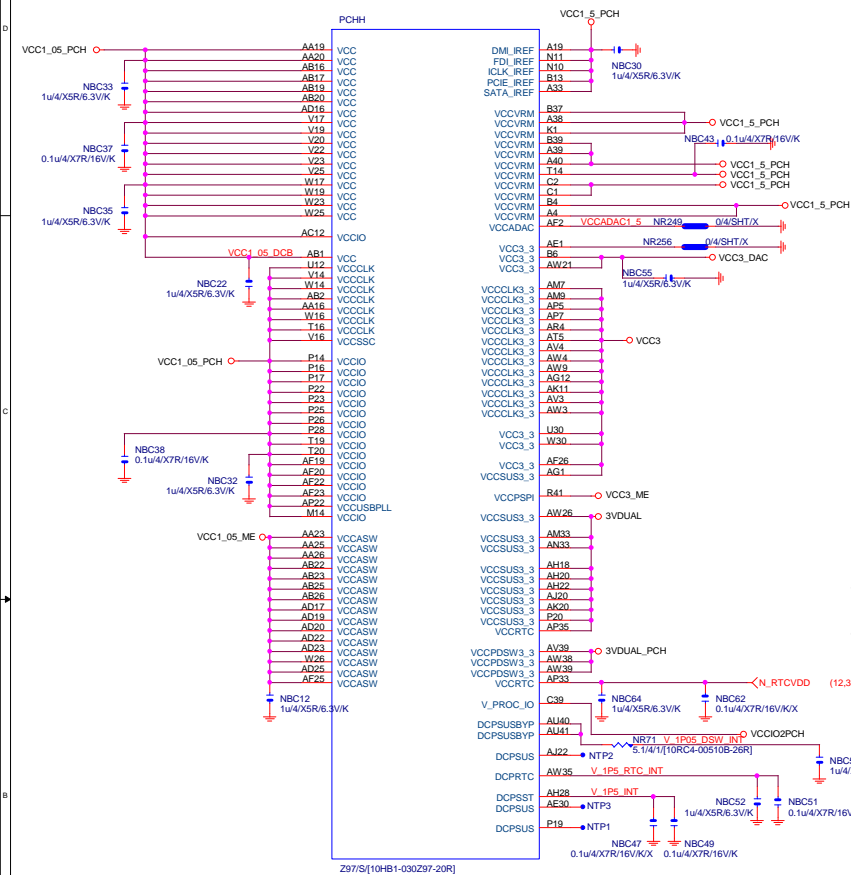
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PCH GPIO , CTRL , AUDIO

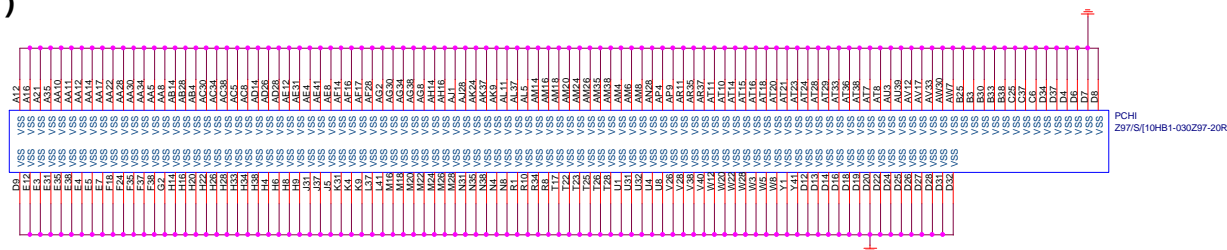
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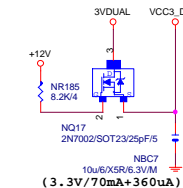
**PCH (H)**



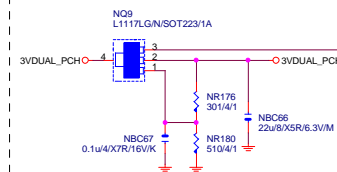
**PCH (I)**



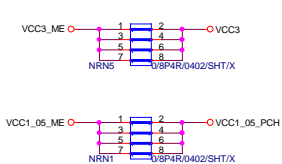
## VCC3\_DAC



## 3VDUAL\_PCH



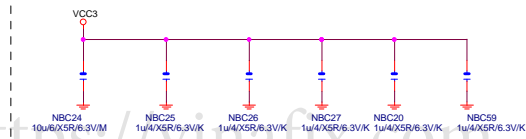
SHT PWR



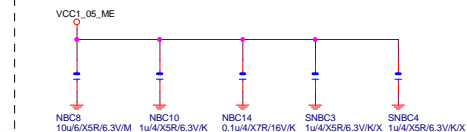
## CAP



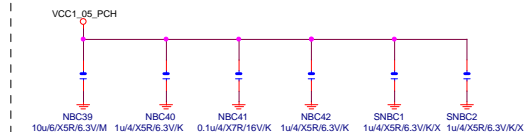
( 3.3V ) ( X6 )



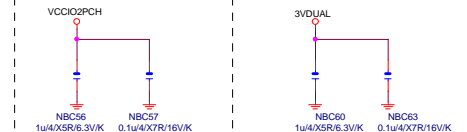
(1.05V) (x5)



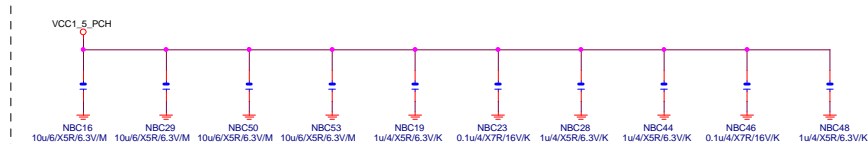
**(1.05V) (X6)**



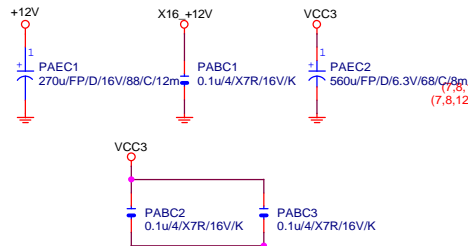
(1.05V)(x2) (3.3V)(x2)



(1.5V) (x10)

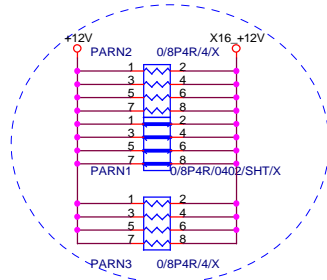


## PCIEX16 CAP



## PCIEX16 PROTECT SHT

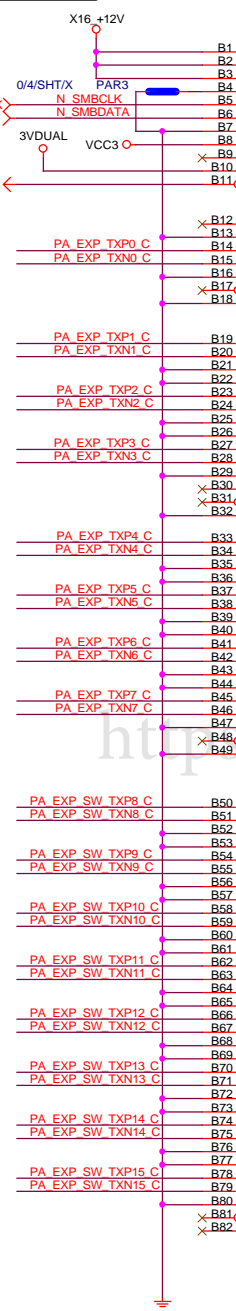
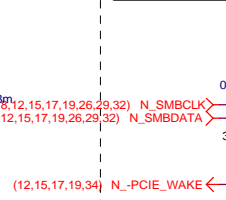
+12 protect short-wire test



## PCIEX16 AC CAP

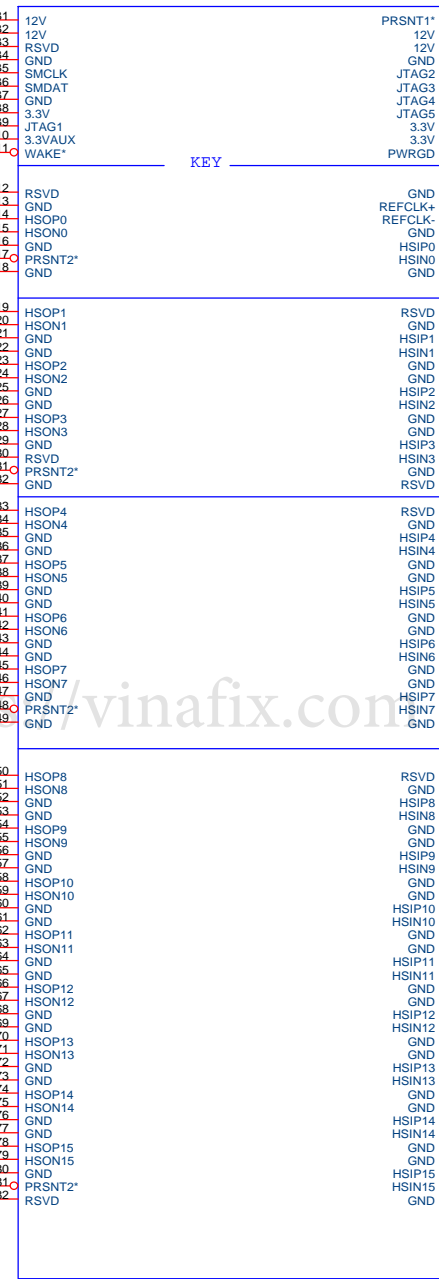
PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP SW TXN15 C

## PCIEX16 SLOT



## PCIESLOT-164DN-Q

3GIO\_\*16



PCI-E/16X-164P/BK/LONG DOUBLE

PCIEX16:16/5/5/5/16

PA EXP RXP0.15]	>>PA_EXP_RXP[0.15] (4,16)
PA EXP RXN0.15]	>>PA_EXP_RXN[0.15] (4,16)
PA EXP TXP0.15]	>>PA_EXP_TXP[0.15] (4,16)
PA EXP TXN0.15]	>>PA_EXP_TXN[0.15] (4,16)
PA EXP SW RXP[8.15]	>>PA_EXP_SW_RXP[8.15] (16)
PA EXP SW RXN[8.15]	>>PA_EXP_SW_RXN[8.15] (16)
PA EXP SW TXP[8.15]	>>PA_EXP_SW_TXP[8.15] (16)
PA EXP SW TXN[8.15]	>>PA_EXP_SW_TXN[8.15] (16)

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

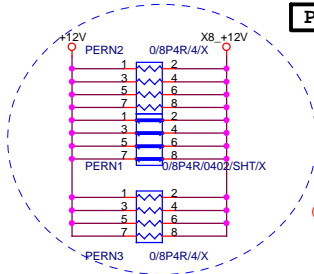
PCI-E REV:2.0--> 5GHZ

Gigabyte Technology

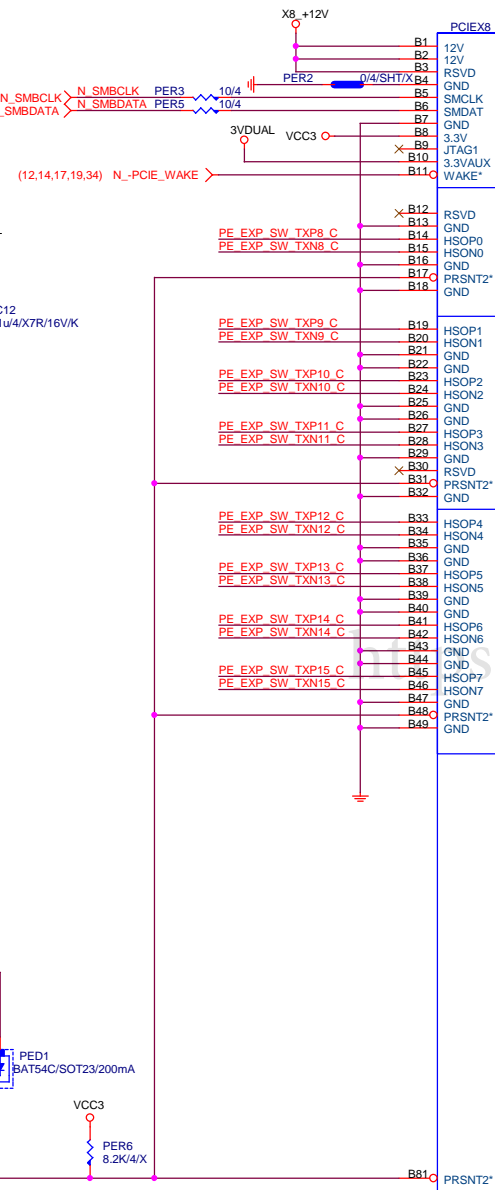
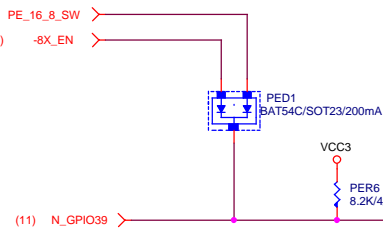
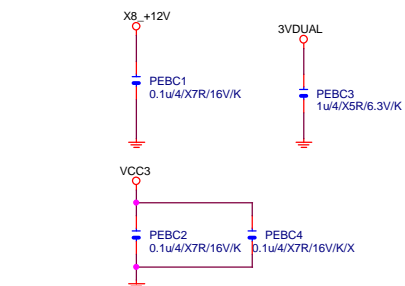
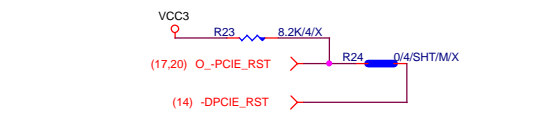
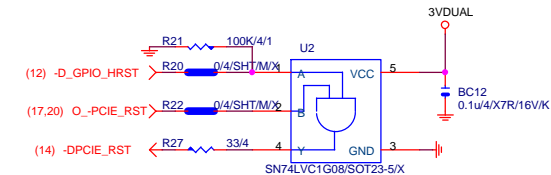
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Document Number			
G1.Sniper Z97			
Date:			
Friday, June 27, 2014			
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14 of 37			
Rev			
1.11			

# PCIEX8 PROTECT SHT

+12 protect  
short-wire  
test



(7,8,12,14,17,19,26,29,32) N\_SMBCLK PER3 10/4  
(7,8,12,14,17,19,26,29,32) N\_SMBDATA PER5 10/4



PCI-E/8X-99P/BK/LONG DOUBLE

PE EXP SW TXP8	PEC2	0.22u4/X5R/6.3V/K	PE EXP SW TXP8 C
PE EXP SW TXN8	PEC3	0.22u4/X5R/6.3V/K	PE EXP SW TXN8 C
PE EXP SW TXP9	PEC4	0.22u4/X5R/6.3V/K	PE EXP SW TXP9 C
PE EXP SW TXN9	PEC5	0.22u4/X5R/6.3V/K	PE EXP SW TXN9 C
PE EXP SW TXP10	PEC6	0.22u4/X5R/6.3V/K	PE EXP SW TXP10 C
PE EXP SW TXN10	PEC7	0.22u4/X5R/6.3V/K	PE EXP SW TXN10 C
PE EXP SW TXP11	PEC8	0.22u4/X5R/6.3V/K	PE EXP SW TXP11 C
PE EXP SW TXN11	PEC9	0.22u4/X5R/6.3V/K	PE EXP SW TXN11 C
PE EXP SW TXP12	PEC10	0.22u4/X5R/6.3V/K	PE EXP SW TXP12 C
PE EXP SW TXN12	PEC11	0.22u4/X5R/6.3V/K	PE EXP SW TXN12 C
PE EXP SW TXP13	PEC12	0.22u4/X5R/6.3V/K	PE EXP SW TXP13 C
PE EXP SW TXN13	PEC13	0.22u4/X5R/6.3V/K	PE EXP SW TXN13 C
PE EXP SW TXP14	PEC14	0.22u4/X5R/6.3V/K	PE EXP SW TXP14 C
PE EXP SW TXN14	PEC15	0.22u4/X5R/6.3V/K	PE EXP SW TXN14 C
PE EXP SW TXP15	PEC16	0.22u4/X5R/6.3V/K	PE EXP SW TXP15 C
PE EXP SW TXN15	PEC17	0.22u4/X5R/6.3V/K	PE EXP SW TXN15 C

Title  
**PCI EXPRESS X 8**

Size  
Custom

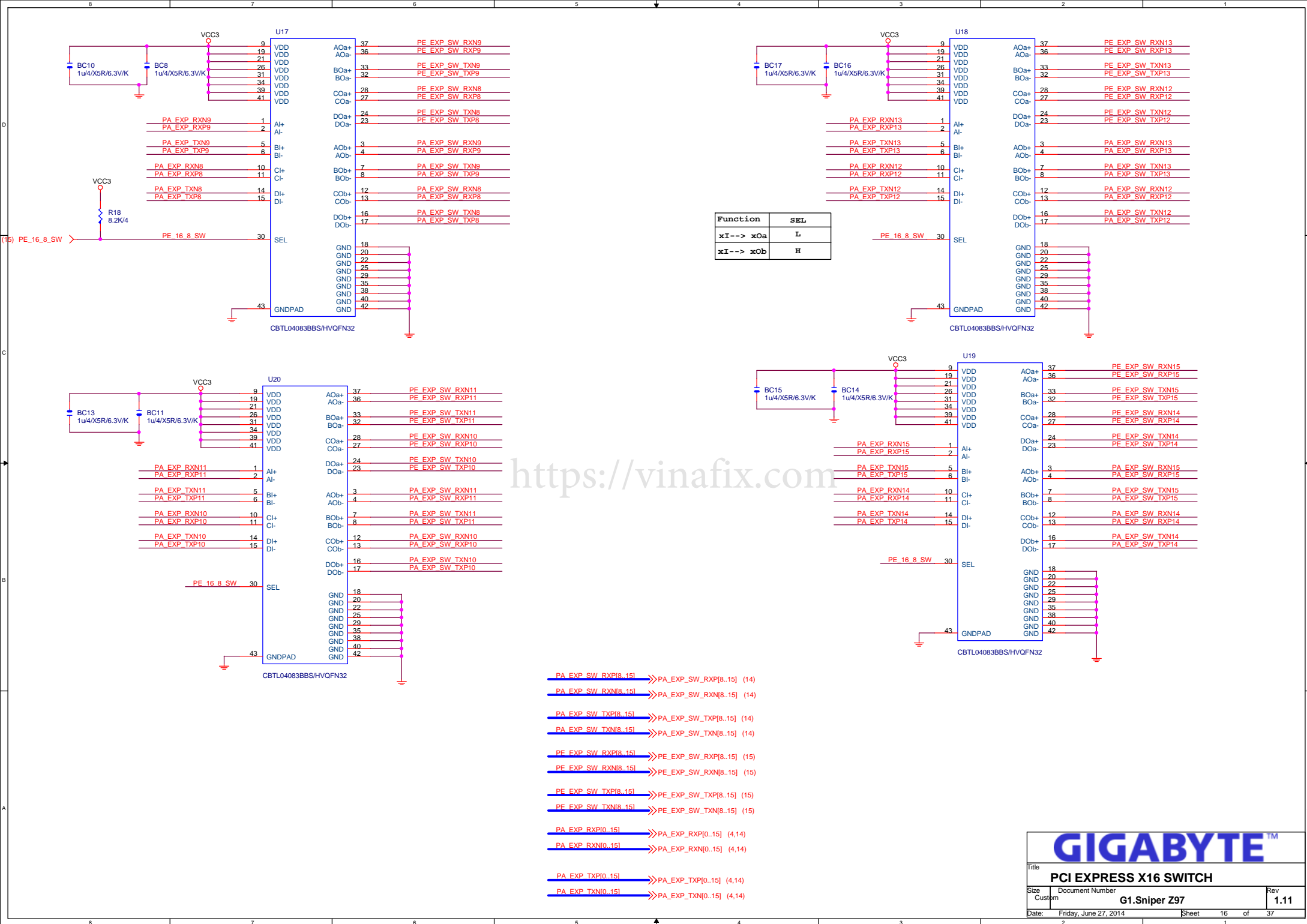
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**G1.Sniper Z97**

Date  
Friday, June 27, 2014

Rev  
**1.11**

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37

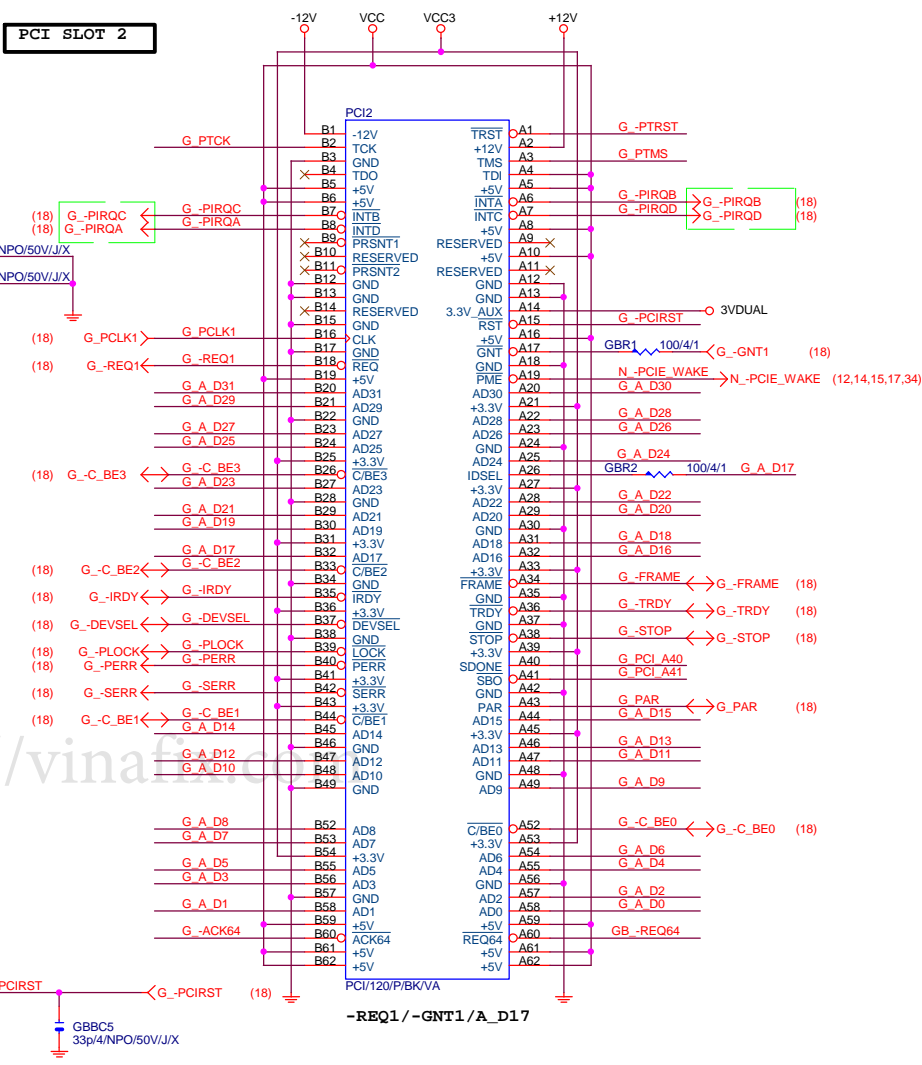
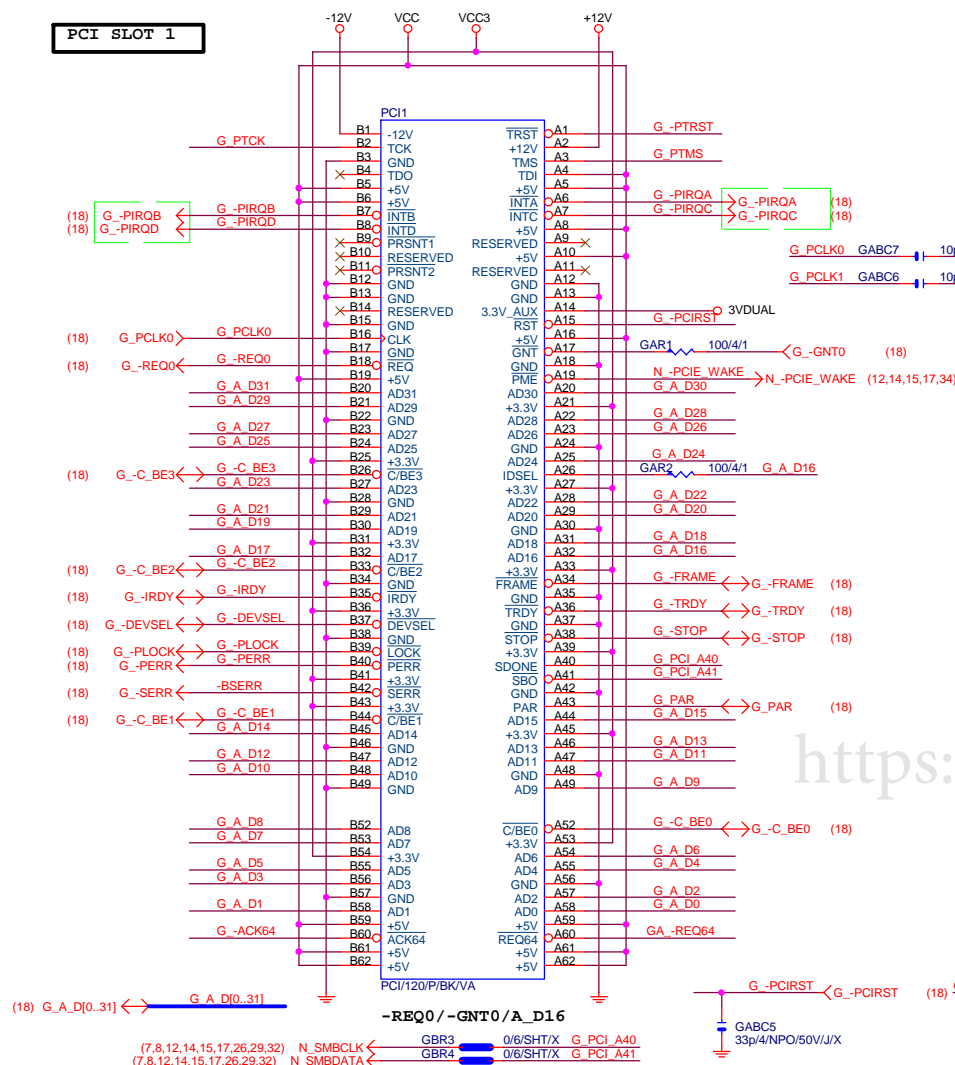






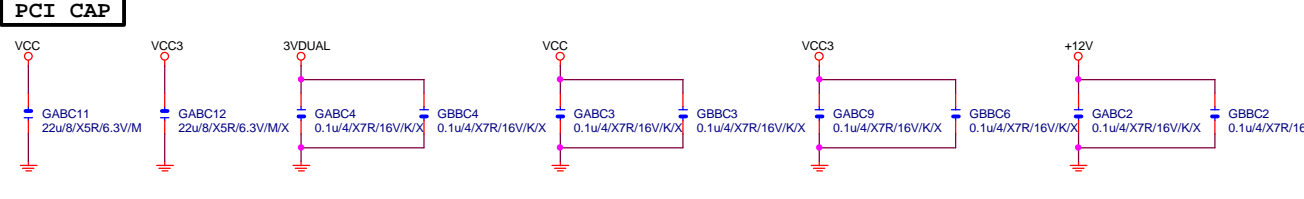
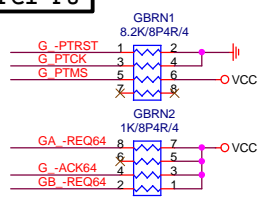
# PCI SLOT 1

# PCI SLOT 2



## PCI PU

## PCI CAP



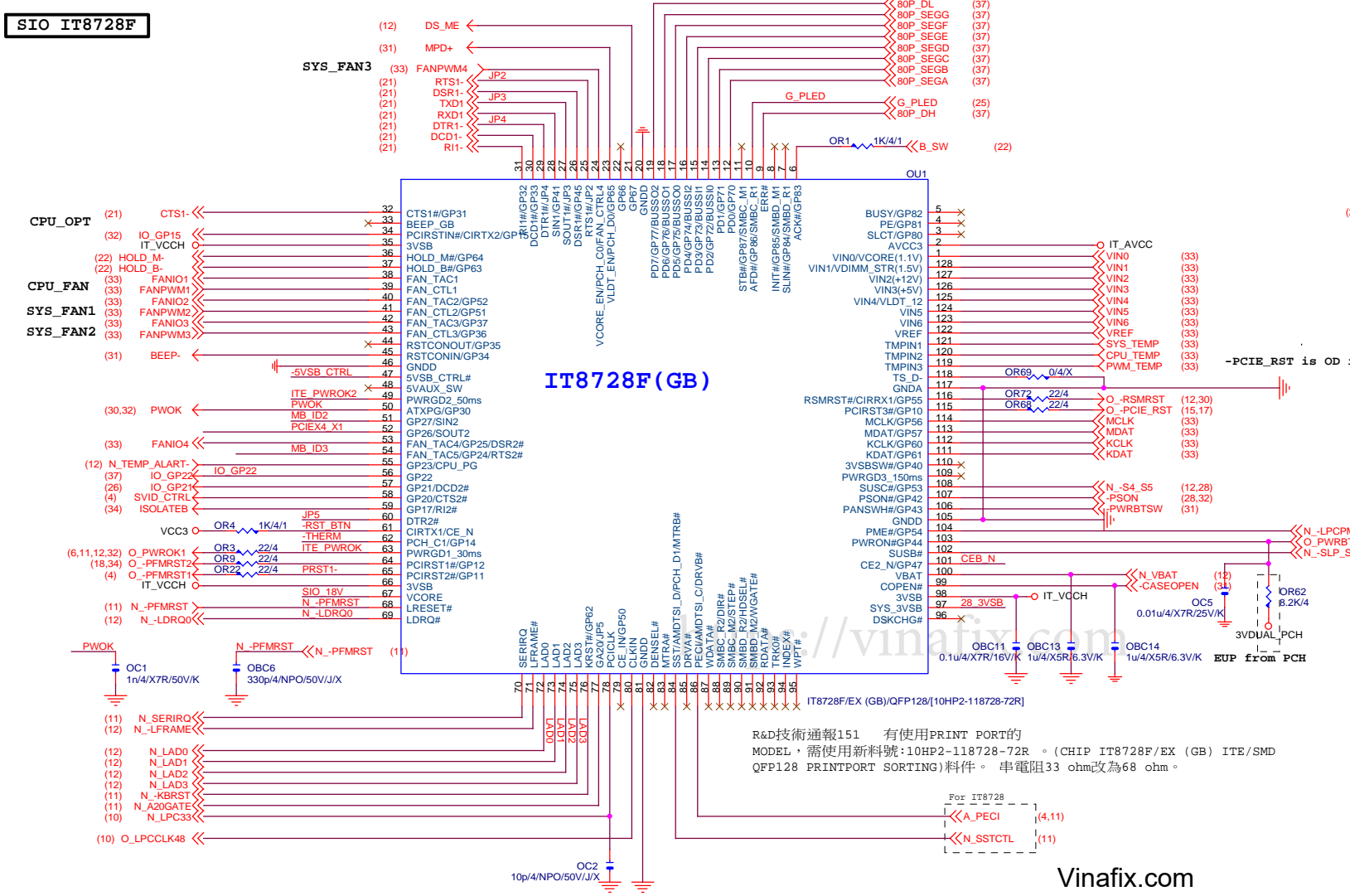
# GIGABYTE™

## PCI SLOT 1&2

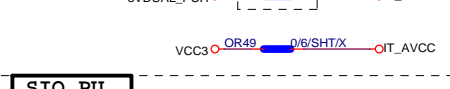
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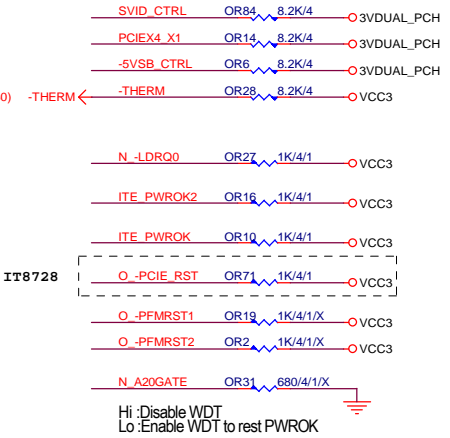
SIO IT8728F



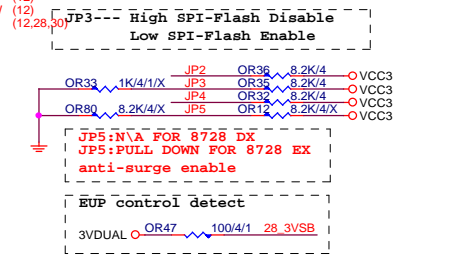
PWR SHT



SIO PU



SIO STRAP

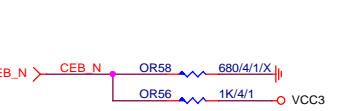


JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

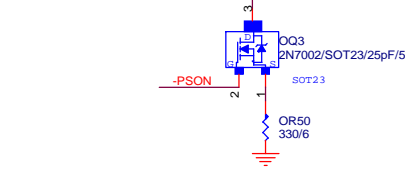
IT8728F NOTE

	IT8728
PIN121	VCORE_EN/PCH_C0
PIN120	VLDI_EN/PCH_D0
PIN19	ATXP6
PIN31	PCH_C1
PIN53	SST/AMDTSI_D/MTRB#/PCH_D1
PIN55	PRCI/AMDTSI_C/DRVB#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VINI/VDIMM_STR(1.5V)
PIN98	VINO/VCORE(1.1V)/NC

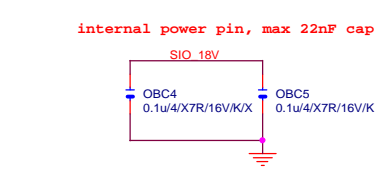
DUAL BIOS OPT STRAP



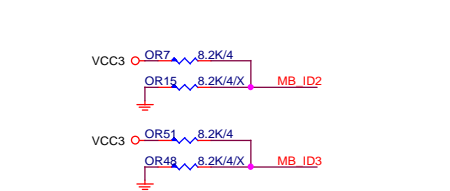
Power leakage



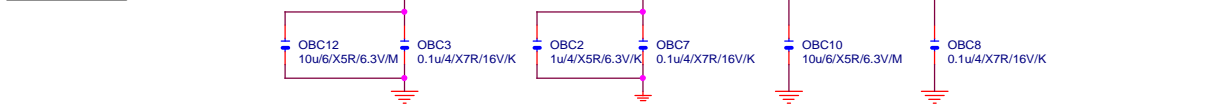
SIO\_18V



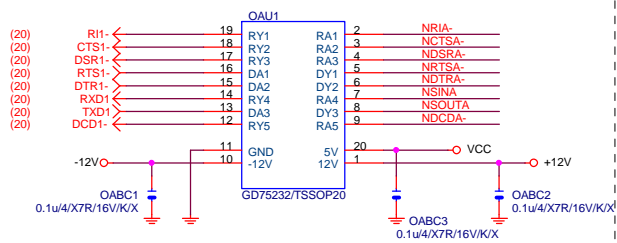
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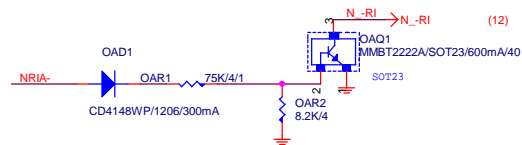
SIO CAP



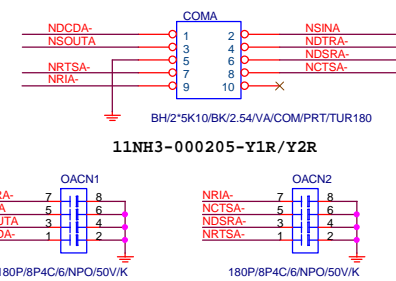
## COMA



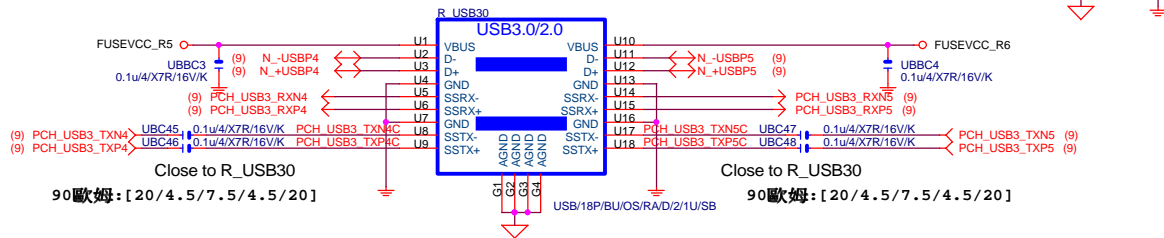
## COM RI



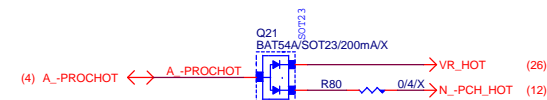
## COM BUFFER



## USB3\_20 CONNECT

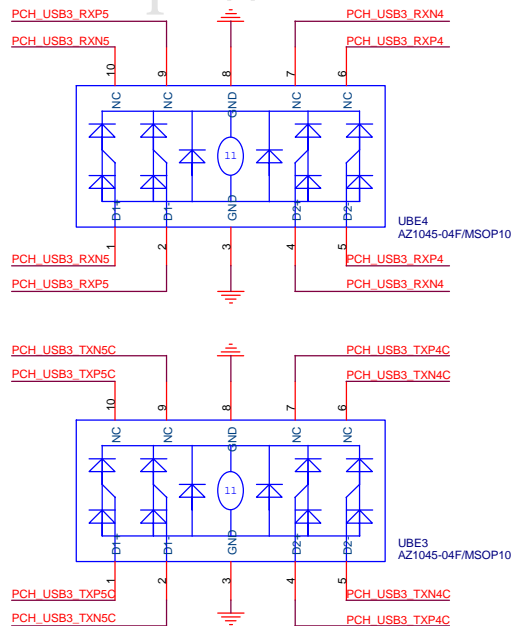


## -PROHOT

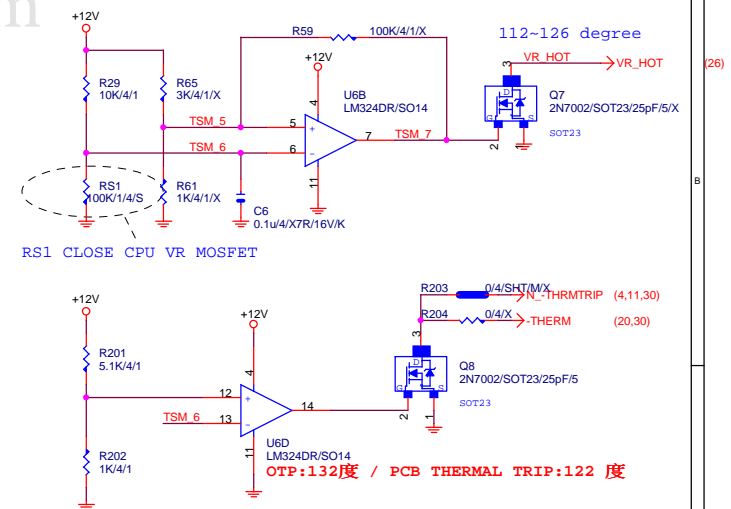


## USB30 ESD PROTECT

<https://vinafix.com>

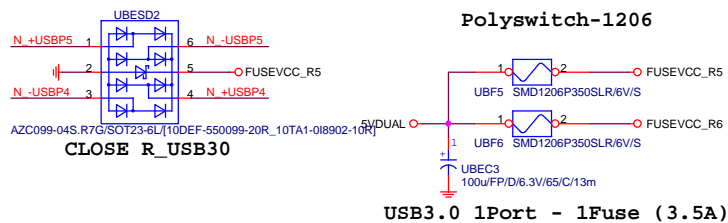


## -PROHOT



## USB20 ESD PROTECT

## USB30 PWR

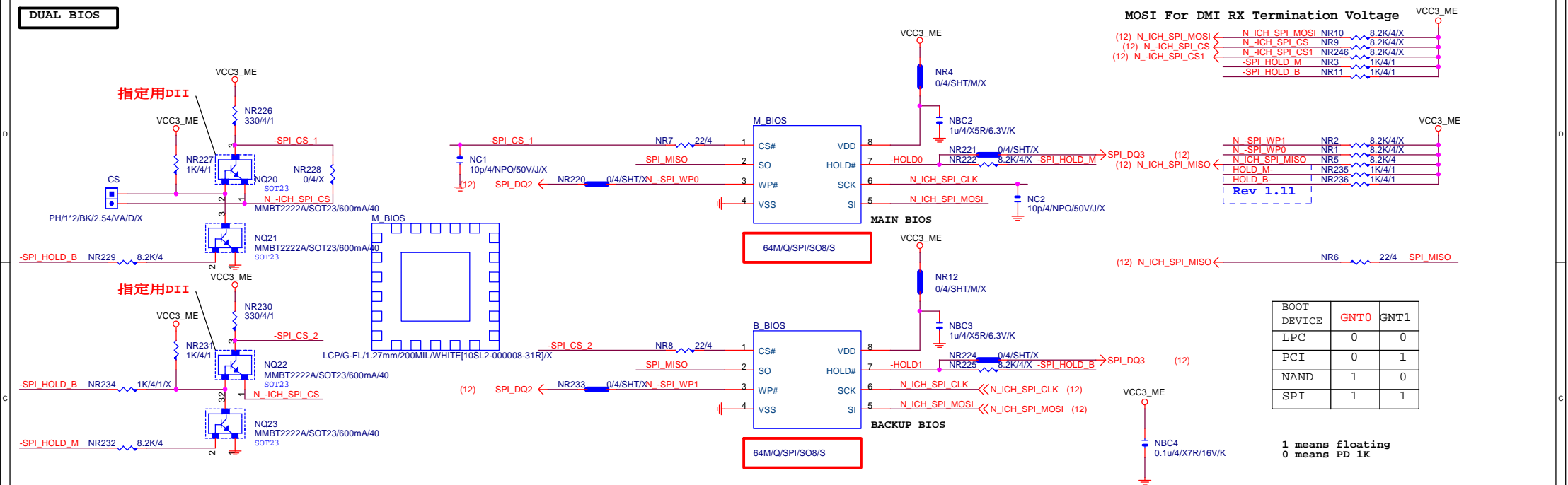


## Gigabyte Technology

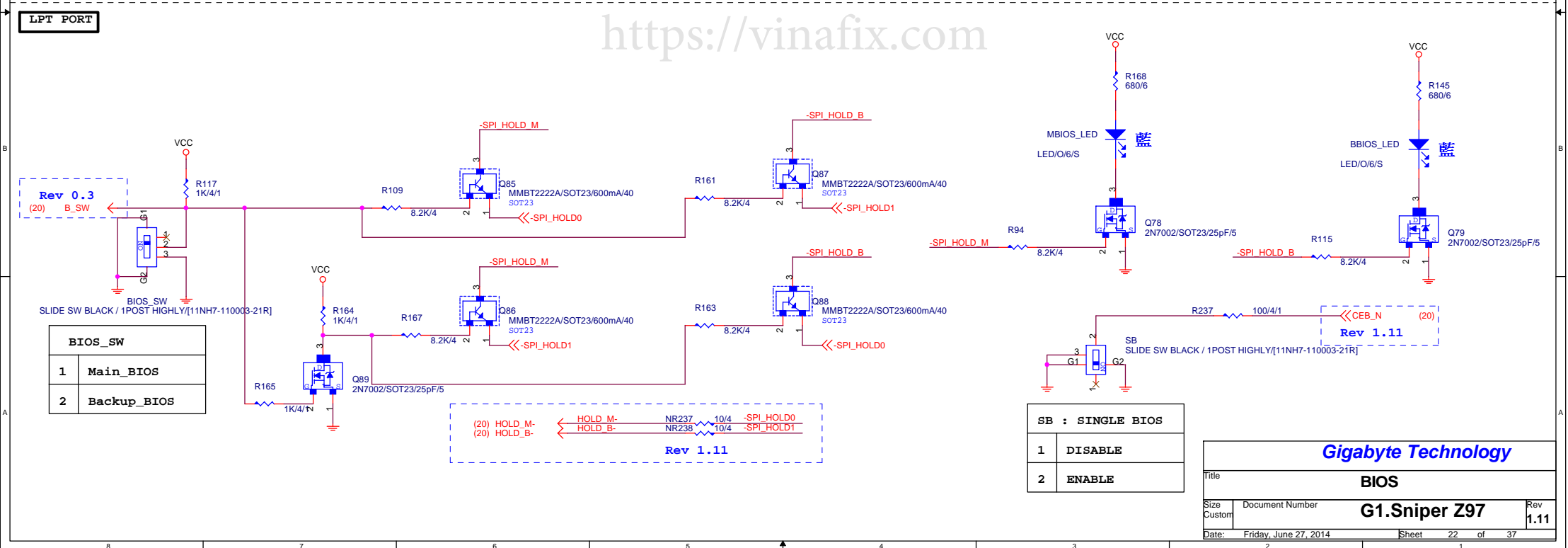
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G1.Sniper Z97

## DUAL BIOS

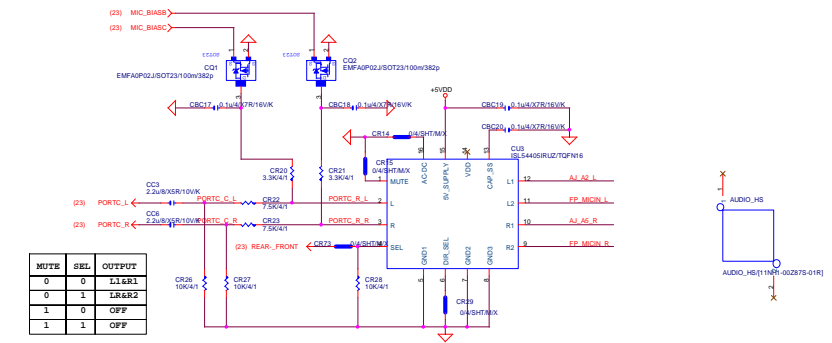


## LPT PORT



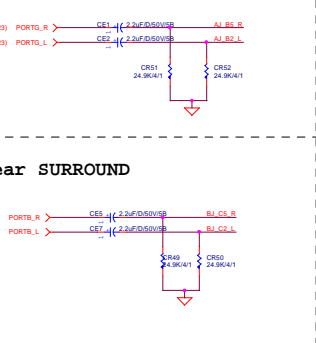


Rear MIC & FP MIC

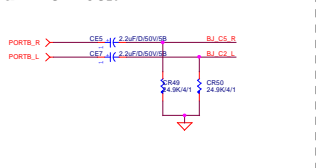


MUTE	SEL	OUTPUT
0	0	L1&R1
0	1	L2&R2
1	0	OFF
1	1	OFF

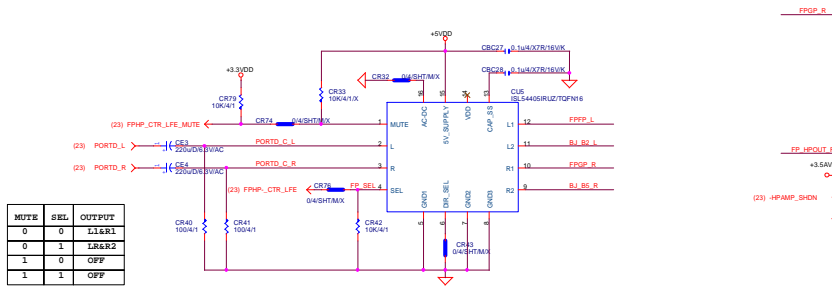
Line-Out



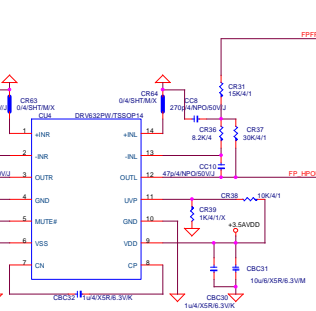
Rear SURROUND



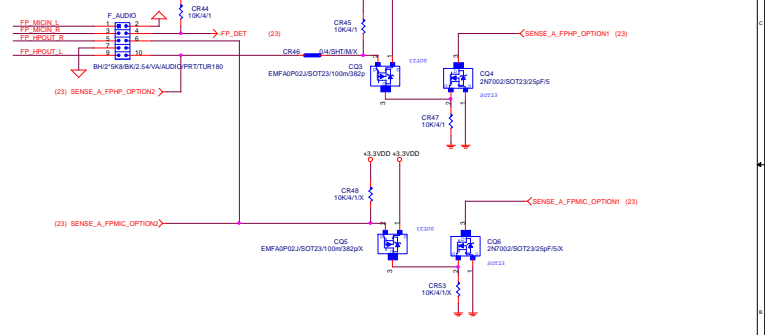
Rear CEN/LFE & FP HP-Out



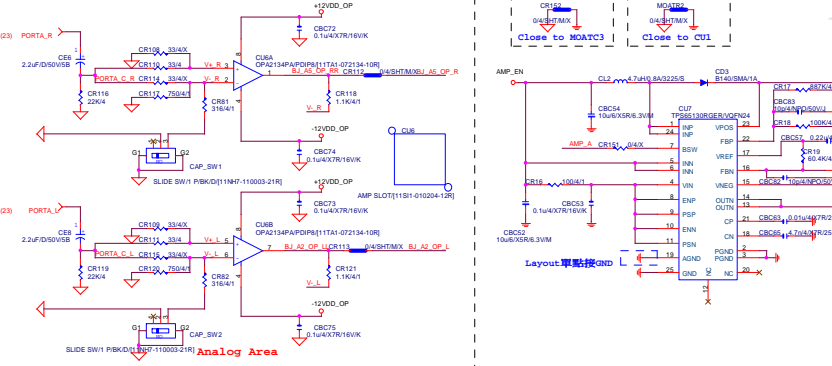
MUTE	SEL	OUTPUT
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0	1	L2&R2
1	0	OFF
1	1	OFF



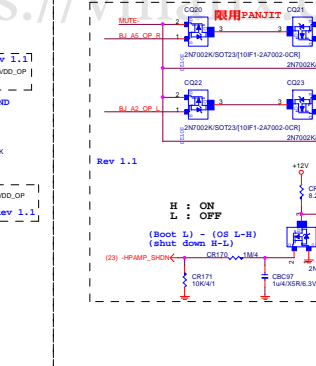
HD Audio FRONT PANEL



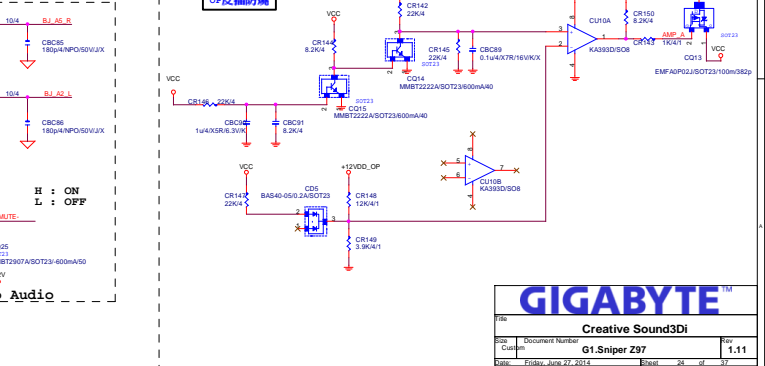
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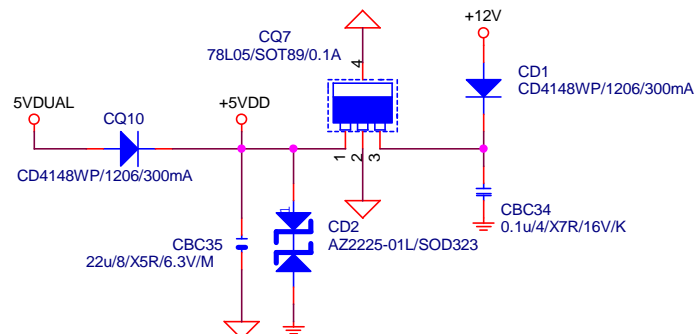
Rev 1.1



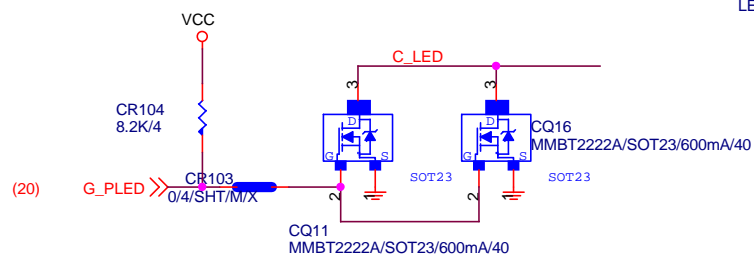
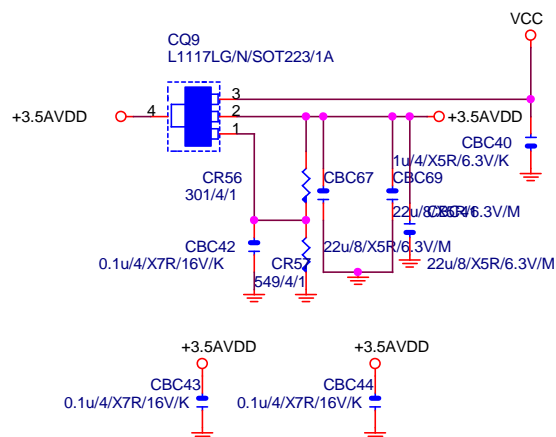
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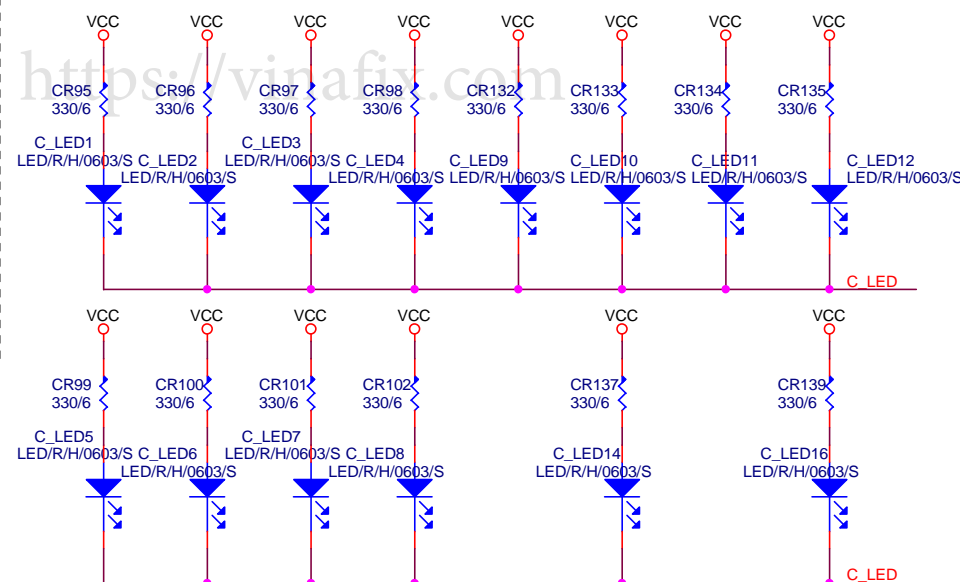
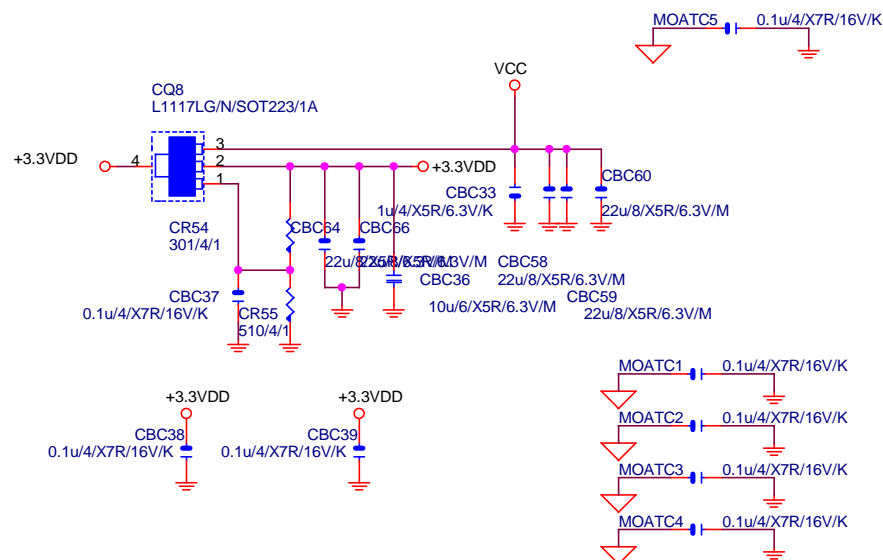
## Switch Power



## Analog Power

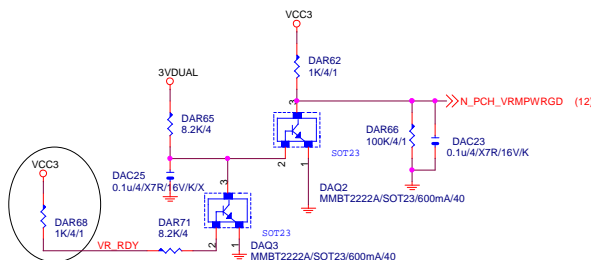
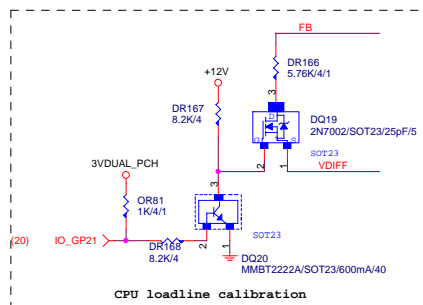
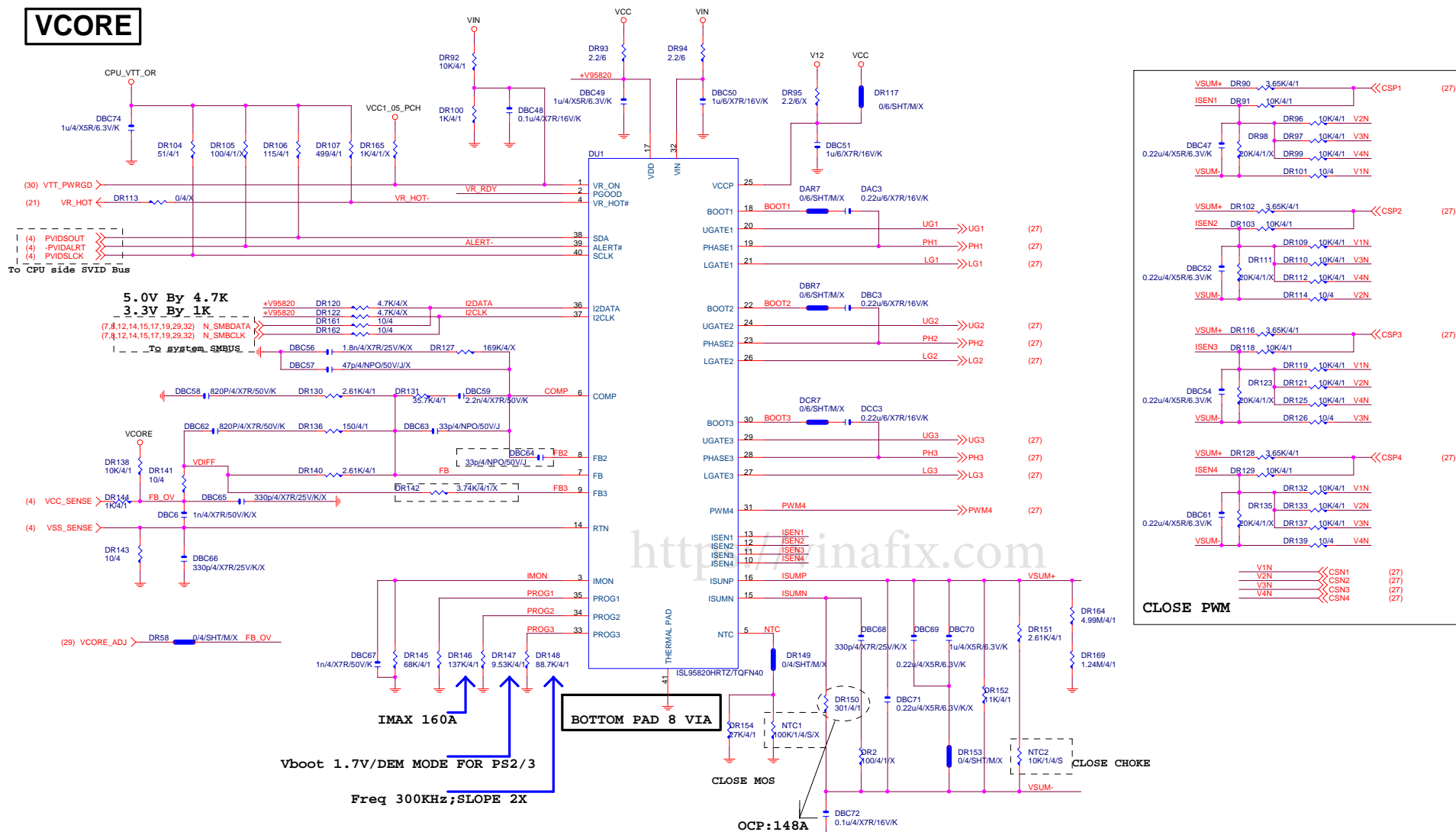


## Digital Power



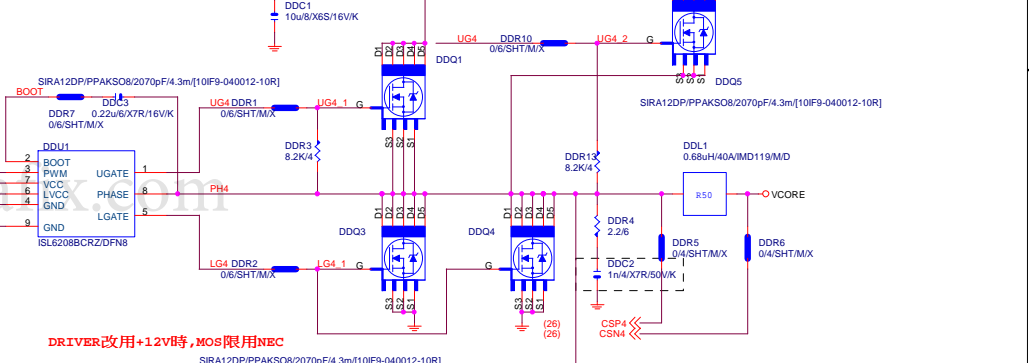
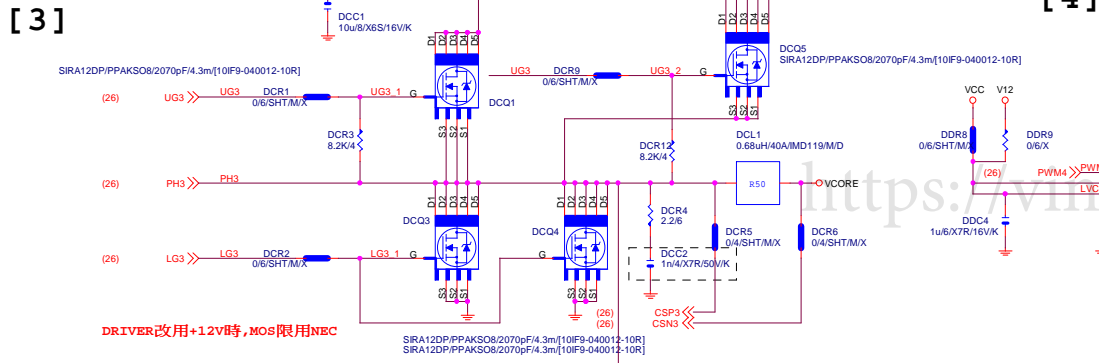
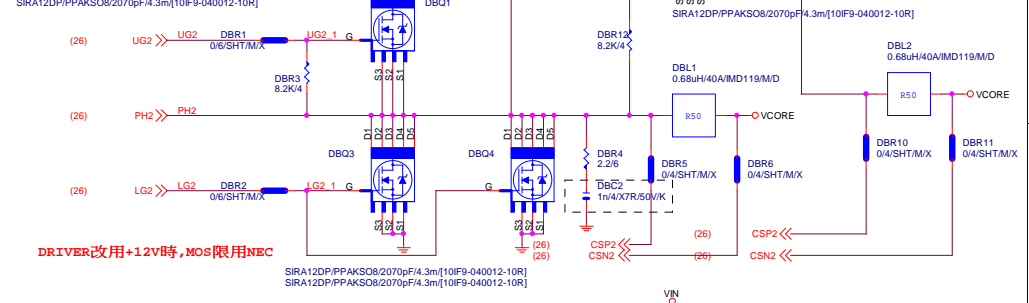
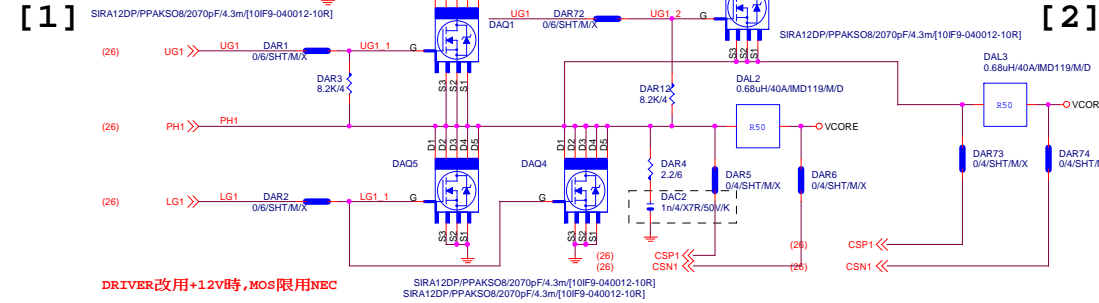
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## VCORE

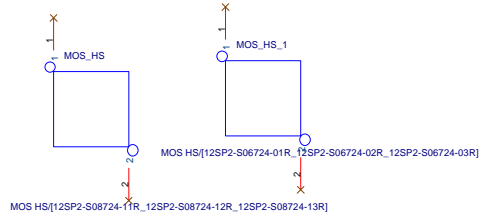


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# VCORE



# MOSFET HEATSINK



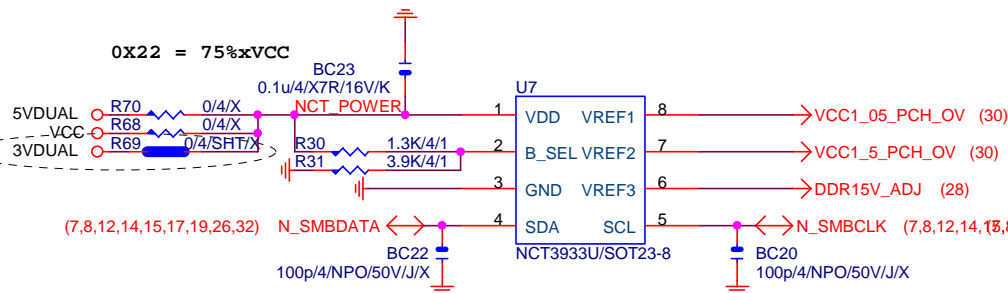
Vinafix.com

Gigabyte Technology

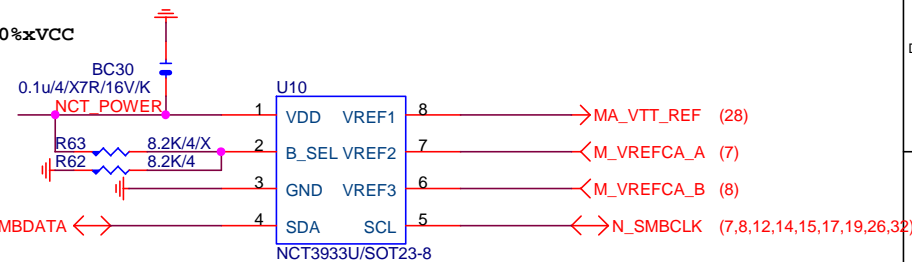
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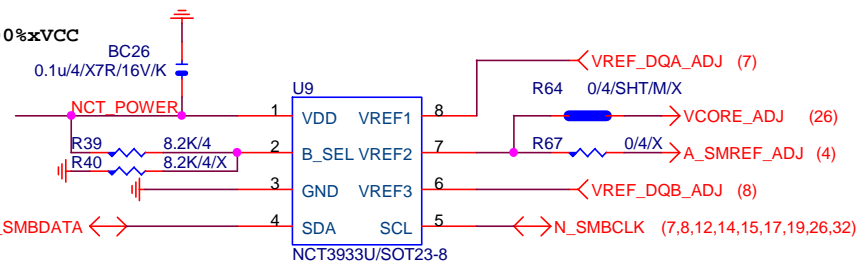
# OVER VOLTAGE



**0X2A = 0%xVCC**



**0X20 = 100%xVCC**



NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

**Gigabyte Technology**

Title			CPU CORE VR-2	
Size Custom			Document Number	
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			Rev 1.11	

**G1.Sniper Z97**

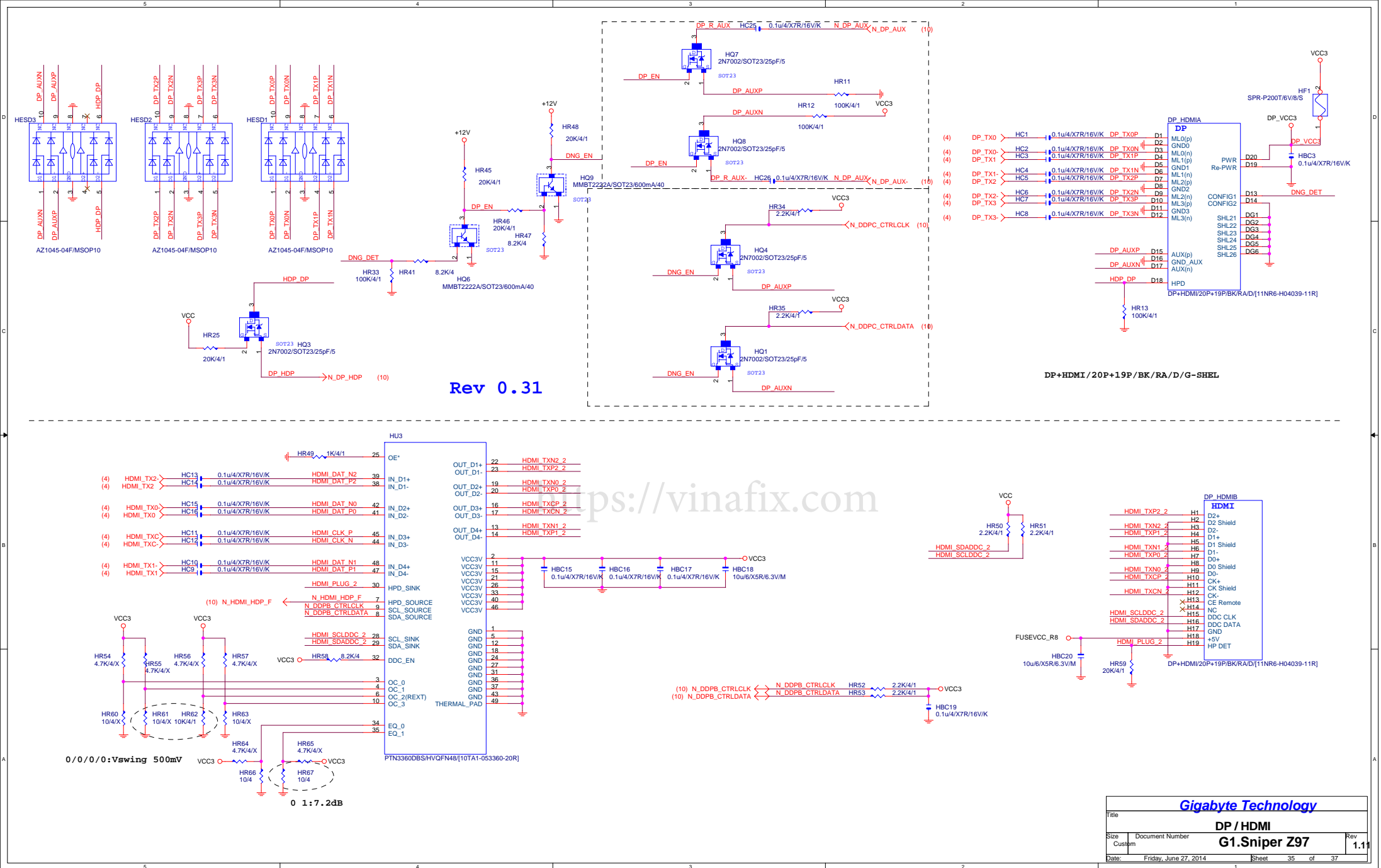










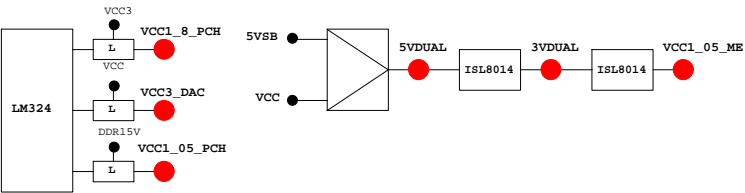


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	PWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

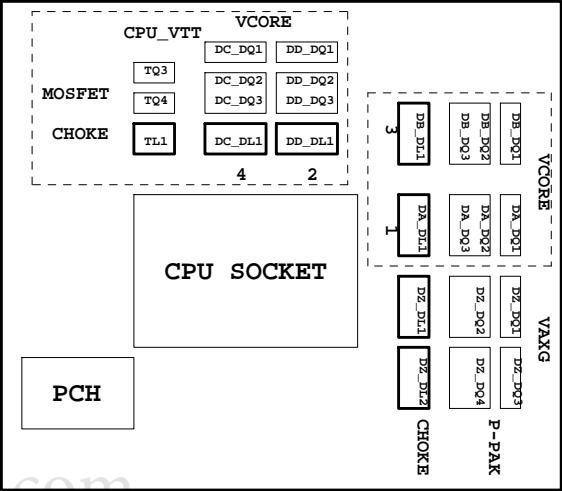
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VBSBW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	SEC_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

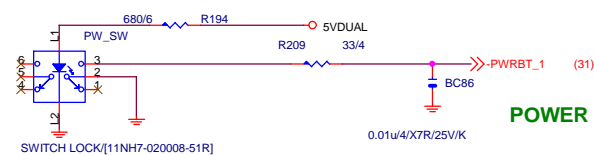
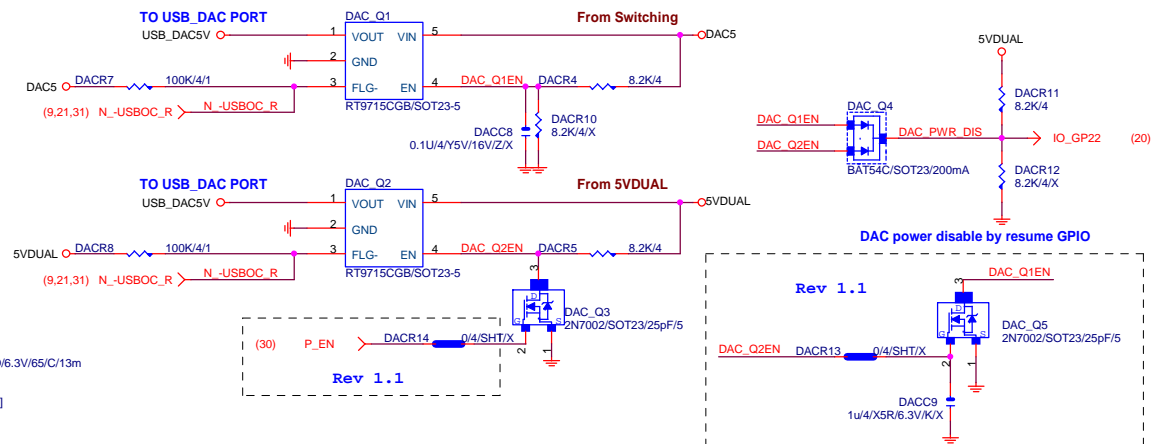
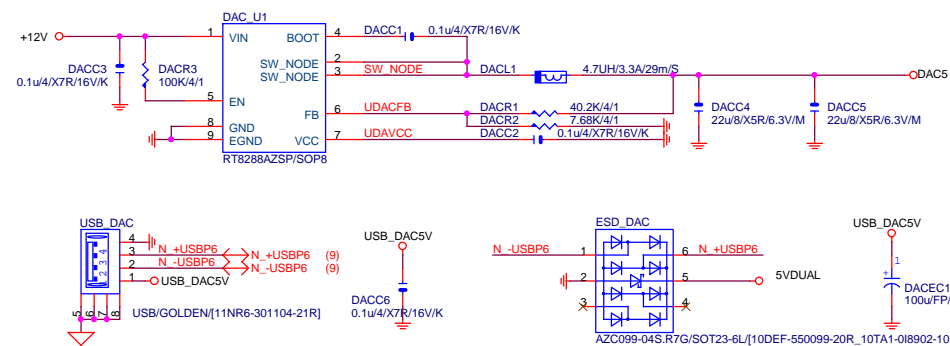
線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

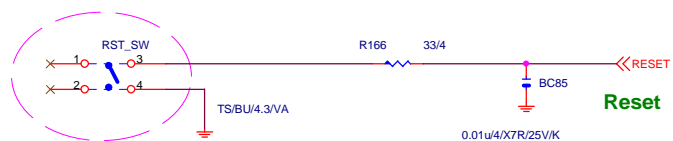
Z77-D3H :  
PCH :  
12SP2-S05511-01R/02R/03R  
MOSFET :  
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

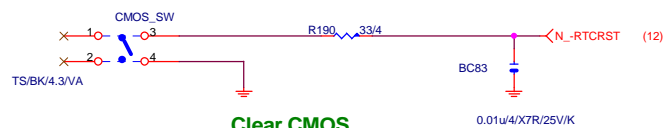
USB\_DAC



## POWER

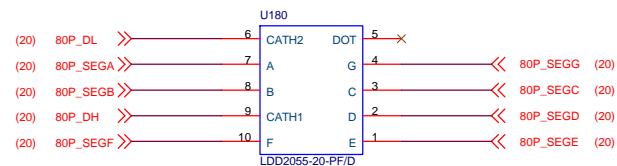
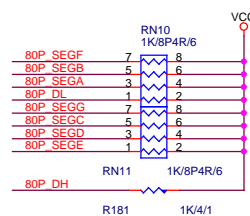


Reset



## Clear CMOS

80 PORT



COMMON CATHODE

